Intel® E7221 Chipset

Datasheet

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Revision History

Rev #	Description	Date
001	Initial Release	September 2004

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Intel® E7221 MCH Features

- Processor Interface
  - —One Intel® Pentium® 4 processor (supports 775-Land package)
  - —Supports Pentium 4 processor FSB interrupt delivery
  - —800 MT/s (200 MHz core) and 533 MT/s (133 MHz core) FSB
  - —Supports Hyper-Threading Technology (HT Technology)
  - —FSB Dynamic Bus Inversion (DBI)
  - —32-bit host addressing for access to 4 GB of memory space
  - —12-deep In-Order Queue
  - —1-deep Defer Queue
  - —GTL+ bus driver with integrated GTL termination resistors
  - —Supports cache line size of 64 bytes

- System Memory
  - —Up to two DDR or DDR2 channels for a total of 4 DIMMs (2 DIMMs / Channel)
  - —Bandwidth up to 8.5 GB/s (DDR2 533 MHz) in dual channel Interleaved mode
  - —Supports standard ECC (Error Correcting Code) x8 only or Non-ECC x8 and x16 DIMMs
  - —Supports asymmetric or interleaved modes
  - —Supports unbuffered DIMMs only
  - —Support for 256 Mb, 512 Mb, and 1 Gb DRAM densities
  - —Opportunistic refresh
  - —Up to 64 simultaneously open pages (four ranks of eight bank devices * 2 channels)
  - —SPD (Serial Presence Detect) scheme for DIMM detection support
  - —Maximum memory size of 4 GB
  - —Supports configurations defined in the JEDEC DDR2 DIMM specification only

- DMI Interface
  - —A chip-to-chip connection interface to Intel® ICH6
  - —2 GB/s point-to-point DMI-ICH6 (1 GB/s each direction)
  - —100 MHz reference clock
  - —32-bit downstream addressing
  - —Messages and error handling

- PCI Express* Interface Support
  - —One x8, x4 or x1 interface
  - —Maximum theoretical aggregate bandwidth of 4 GB/s when x8
  - —Compatible with the PCI Express Base Specification Revision 1.0a

- Package
  - —1210 balls, 37.5 mm x 37.5 mm, variable ball pitch

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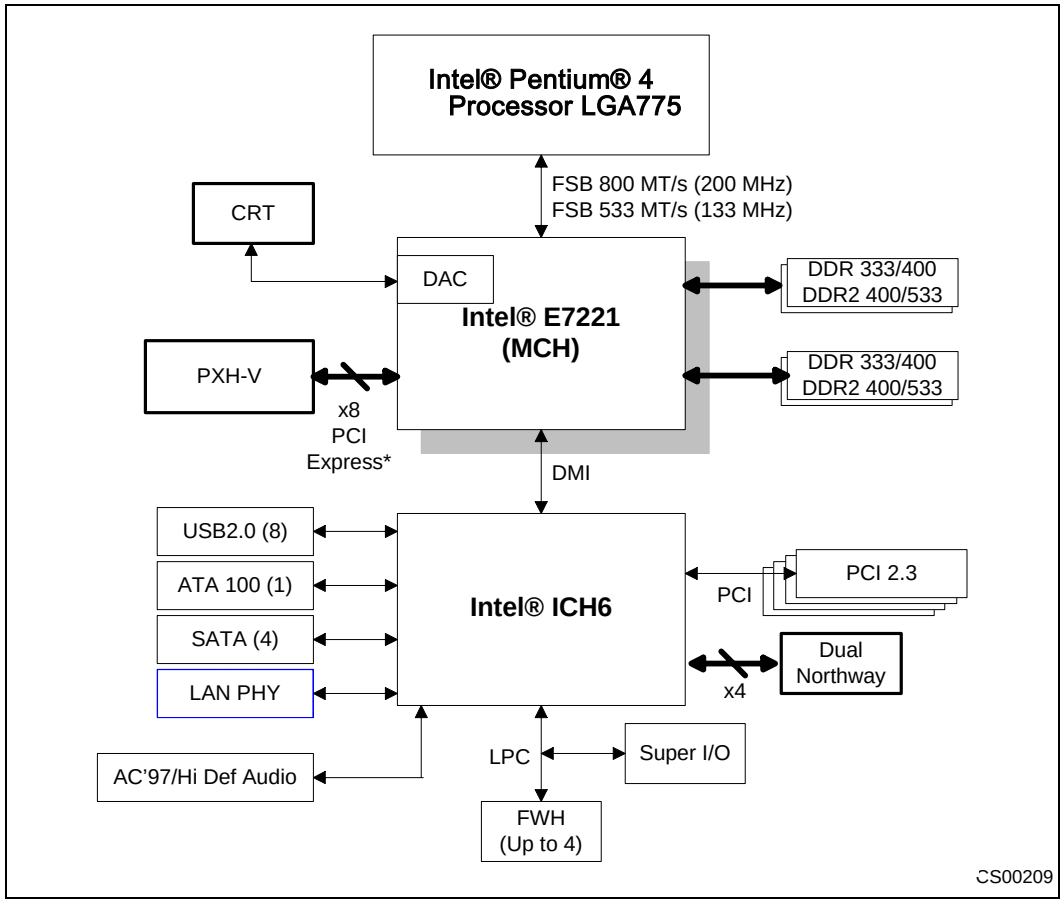
1 Introduction

The Intel® E7221 chipset is targeted for the UP sub-value entry server market and consists of the following components: Memory Controller Hub (MCH), Intel® 6702PXH 64-bit PCI Hub (PCI Express x8 equivalent), and Intel® I/O Controller Hub 6 (ICH6). In addition, the MCH includes Integrated Graphics with standard SVGA capabilities.

This document is the datasheet for the Intel® E7221 MCH. Topics covered include; signal description, system memory map, register descriptions, a description of the MCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

Note: Unless otherwise specified, ICH6 refers to the Intel® 82801FB ICH6, 82801FR ICHR, 82801FW ICH6W, and 82801FRW ICH6RW I/O Controller Hub components.

Figure 1-1. Intel® E7221 Chipset System Block Diagram Example



1.1 Terminology

Term	Description
Core	The internal base logic in the chipset.
DBI	Dynamic Bus Inversion; DBI limits the number of data signals that are driven to a low voltage on each quad-pumped data phase.
DDR	Double Data Rate DRAM memory technology
DDR2	A second generation Double Data Rate DRAM memory technology.
DMI	Chipset-ICH Direct Media Interface
ECC	Error Correcting Code
FSB	Front Side Bus, synonymous with Host or processor bus.
Full Reset	Full reset is when PWROK is deasserted. Warm reset is when both RSTINB and PWROK are asserted.
Host	This term is used synonymously with “processor”.
INTx	An interrupt request signal where x stands for interrupts A, B, C, and D.
IGD	Internal Graphics Device
Intel® ICH6	Sixth generation I/O Controller Hub component that contains additional functionality compared to previous ICHs.
MCH	Memory Controller Hub component that contains the processor interface, DRAM controller, and Intel® 6702PXH 64-bit PCI Hub interface. It communicates with the I/O controller hub (ICH6) and other I/O controller hubs over the DMI interconnect. Throughout this document, MCH refers to the Intel® E7221 MCH, unless otherwise specified.
MSI	Message Signaled Interrupt. A transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
PCI Express	Third Generation Input Output called (PCI Express). A high-speed serial interface in which the configuration is software compatible with the existing PCI specifications. The specific PCI Express implementation intended for connecting the MCH, ICH6, and Intel® 6702PXH 64-bit PCI Hub controllers.
Primary PCI	The physical PCI Bus that is driven directly by the ICH6 component. Communication between PCI_A and the chipset occurs over DMI. Note that even though the Primary PCI Bus is referred to as PCI_A, it is not PCI Bus 0 from a configuration standpoint.
Intel® 6702PXH 64-bit PCI Hub	The Intel® 6702PXH 64-bit PCI Hub provides connection between the MCH x8 PCI Express port and a single independent PCI or PCI-X Bus interface. The Intel® 6702PXH 64-bit PCI Hub provides configuration support for 32 or 64 bit PCI devices operating at 33 MHz, 66 MHz, 100 MHz, or 133 MHz.
SEC	Single-bit Error Correct
SCI	System Control Interrupt. Used in ACPI protocol.
SERR	System Error. An indication that an unrecoverable error has occurred on an I/O bus.
SMI	System Management Interrupt. Used to indicate any of several system conditions such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity.
Rank	A unit of DRAM corresponding to eight x8 DRAM devices in parallel or four x16 DRAM devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DIMM.
TOLM	Top Of Low Memory. The highest address below 4GB for which a processor initiated memory read or write transaction will create a corresponding cycle to DRAM on the memory interface.
VCO	Voltage Controlled Oscillator

1.2 Reference Documents

Title	Version	Reference # / Availability
Intel® E7221 Chipset Thermal Design Guide		
Advanced Configuration and Power Interface Specification	2.0b	http://www.acpi.info
The PCI Local Bus Specification	2.3	http://www.pcisig.com/specifications
PCI Express Specification	1.0a	http://www.pcisig.com/specifications

1.3 MCH Overview

The MCH connects to the processor as shown in Figure 1-1. A major role of the MCH in a system is to manage the flow of information between its interfaces: the processor interface (FSB), the System Memory interface (DRAM controller), the Intel® 6702PXH 64-bit PCI Hub interface via PCI Express, and the I/O Controller Hub through the DMI interface. This includes arbitrating between the interfaces when each initiates transactions. The processor interface supports the Pentium 4 processor subset of the Extended Mode of the Scalable Bus Protocol.

The MCH supports up to two channels of DDR or DDR2 SDRAM. The MCH also supports the PCI Express based Intel® 6702PXH 64-bit PCI Hub. Thus, the E7221 chipset is NOT compatible with AGP (1X, 2X, 4X, or 8X).

To increase system performance, the MCH incorporates several queues and a write cache. The MCH also contains advanced power management logic.

1.3.1 Host Interface

The MCH is optimized for the Pentium 4 processors in the LGA775 socket. The MCH can use a single FCmPGA4 socket processor. The MCH supports FSB frequencies of 200 MHz (800 MT/s) and 133 MHz (533 MT/s) using a scalable FSB. The MCH supports the Pentium 4 processor subset of the Extended Mode Scalable Bus Protocol. The primary enhancements over the Compatible Mode P6 bus protocol are: Source synchronous double-pumped (2x) Address and Source synchronous quad-pumped (4x) Data.

The MCH supports 32-bit host addressing, decoding up to 4 GB of the processor's memory address space. Host-initiated I/O cycles are decoded to PCI Express, DMI, or the MCH configuration space. Host-initiated memory cycles are decoded to PCI Express, DMI, or system memory. PCI Express device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from PCI Express using PCI semantics and from DMI to system memory will be snooped on the host bus.

1.3.2 System Memory Interface

The MCH integrates a system memory DDR/DDR2 controller with two, 64-bit (non-ECC) or 72-bit (ECC) wide interfaces. Only Double Data Rate (DDR/DDR2) memory is supported; consequently, the buffers support only SSTL_2 (2.6V)/1.8V signal interfaces. The memory controller interface is fully configurable through a set of control registers. Features of the MCH memory controller include:

- The MCH System Memory Controller directly supports one or two channels of memory, 64-bit (non-ECC) or 72-bit (ECC) wide interfaces.
- Supports two memory addressing organization options:
  - — Asymmetric: “Stacked” channels are assigned addresses serially. Channel B addresses are assigned after all Channel A addresses
  - — Interleaved: Addresses are ping-ponged between the channels after each cache line (64B boundary)
- Supports maximum memory bandwidths:
  - — 4.2 GB/s in Single Channel or Dual Channel Asymmetric mode
  - — 6.4 GB/s in Dual Channel Interleaved Mode assuming DDR2 400 MHz
  - — 8.5 GB/s in Dual Channel Interleaved Mode assuming DDR2 533 MHz
- Supports DDR memory DIMM frequencies of 333 MHz and 400 MHz or DDR2 memory DIMM frequencies of 400 MHz and 533 MHz. The speed used in all channels is the speed of the slowest DIMM in the system.
- I/O Voltage of 2.6V for DDR, and 1.8V for DDR2
- Directly supports only one or two channels of ECC or non-ECC DDR2 DIMMs
- Supports 256-Mb, 512-Mb, and 1-Gb DRAM densities
- Supports unbuffered DIMMs only
- Supports opportunistic refresh
- Supports up to 64 simultaneous open pages in dual channel mode (assuming 4 ranks of 8i devices)
- Supports Fast Chip Select mode
- Supports Partial Writes to memory using Data Mask (DM) signals
- Supports page sizes of 4KB, 8KB, and 16KB
- For standard ECC DIMMs:
  - — Supports DDR devices using x8 or x16 DRAM technologies
  - — Supports DDR2 devices using only x8 DRAM technologies
- For non-ECC DIMMs:
  - — Supports DDR/DDR2 devices using x8 or x16 DRAM technologies

The MCH supports a memory thermal management scheme to selectively manage reads and/or writes. Memory thermal management can be triggered either by on-die thermal sensor, or by preset limits. Management limits are determined by weighted sum of various commands that are scheduled on the memory interface.

1.3.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the MCH and ICH6. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

To provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the ICH6 supports two virtual channels on DMI: VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (i.e., the ICH6 and MCH). Features of the DMI include:

- A chip-to-chip connection interface to ICH6
- 2 GB/s (1 GB/s in each direction) point-to-point DMI interface to ICH6
- 100 MHz reference clock (shared with PCI Express Interface)
- 32-bit downstream addressing
- APIC and Message Signaled Interrupt (MSI) messaging support; will send Intel-defined “End Of Interrupt” broadcast message when initiated by the processor
- SMI, SCI, and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters

1.3.4 PCI Express* Interface (Intel® 6702PXH 64-bit PCI Hub Interface)

The MCH contains a 8-lane (x8) PCI Express* port designed for the Intel® 6702PXH 64-bit PCI Hub component. The interface is compatible with the PCI Express Base Specification Revision 1.0a. The x8 port operates at a frequency of 2.5 Gb/s on each lane while employing 8b/10b encoding, and supports a maximum theoretical realized aggregate bandwidth is 4 GB/s when in x8 mode. Features of the PCI Express Interface include:

- Fully compliant to the *PCI Express Base Specification*, Rev 1.0a
- Theoretical PCI Express transfer rate of 2.5 Gb/s
- Raw bit rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface
- Maximum theoretical realized bandwidth on interface of 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s when x8
- PCI Express Extended Configuration Space. The first 256 bytes of configuration space alias directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express Enhanced Addressing Mechanism accesses the device configuration space in a flat memory mapped fashion
- Automatic discovery, negotiation, and training of link out of reset
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, Intel® 6702PXH 64-bit PCI Hub Relaxed ordering)

- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., normal PCI 2.3 configuration space as a PCI-to-PCI bridge)
- PCI Express Interface supports one x8-lane port that can also be configured as a single x1 or x4 lane port
- Intel® 6702PXH 64-bit PCI Hub Rev. 1.0 compliant

1.3.5 Integrated Graphics

The Intel® E7221 MCH includes an integrated graphics engine that supports standard SVGA drivers with analog display capabilities.

1.3.6 System Interrupts

The MCH interrupt support includes:

- Supports both the Intel® 8259 and Pentium® 4 processor FSB interrupt delivery mechanisms
- Supports interrupts signaled as upstream Memory Writes from PCI Express and DMI
  - — MSIs routed directly to FSB
  - — From IOxAPICs
- Provides redirection for IPI (interprocessor interrupts) and upstream interrupts to the FSB

1.3.7 MCH Clocking

The differential FSB clock (HCLKP/HCLKN) is set to either 133 MHz or 200 MHz, this supports FSB transfer rates of 533 MT/s or 800 MT/s, respectively. The Host PLL generates 2X, 4X, and 8X versions of the host clock for internal optimizations. The MCH core clock is synchronized to the host clock.

The internal and external memory clocks of 133 MHz and 200 MHz are generated from one of two MCH PLLs that use the host clock as a reference. This includes 2X and 4X for internal optimizations.

The PCI Express core clock of 250 MHz is generated from a separate PCI Express PLL. This clock uses the fixed 100 MHz Serial Reference Clock (GCLKP/GCLKN) for reference.

All of the above mentioned clocks are capable of tolerating Spread Spectrum clocking as defined in the Clock Generator specification. Host, Memory, and PCI Express x8 PLLs, and all associated internal clocks are disabled until PWROK is asserted.

1.3.8 Power Management

MCH Power Management support includes:

- SMRAM space remapping to A0000h (128KB)
- Supports extended SMRAM space above 256 Mb, additional 1 Mb TSEG from the base of graphics stolen memory (BSM) when enabled, and cacheable (cacheability controlled by the processor)
- ACPI Rev 1.0 compliant power management
- Supports processor states C0, C1, C2, C3, and C4
- Supports system states: S0, S1, S4, and S5
- Supports processor thermal management 2 (TM2)
- Microsoft Windows NT* Hardware Design Guide v1.0 compliant

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2 Signal Description

This section provides a detailed description of MCH signals. The signals are arranged in functional groups according to their associated interface. The states of all of the signals during reset are provided in Section 2.10.

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bidirectional Input/Output pin
GTL+	Open Drain GTL+ interface signal. Refer to the *GTL+ I/O Specification* for complete details. The MCH integrates GTL+ termination resistors, and supports VTT of from 0.83 V to 1.65 V (including guardbanding).
PCIE	PCI Express interface signals. These signals are compatible with *PCI Express Specification*, Rev 1.0a, signaling environment AC specifications and are AC coupled. The buffers are not 3.3V tolerant. Differential voltage specification = (|D+ – D–|) • 2 = 1.2V max. Single-ended maximum = 1.5V Single-ended minimum = 0V.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 V max. Single-ended maximum = 1.5 V Single-ended minimum = 0 V.
CMOS	CMOS buffers. 1.5V tolerant.
COD	CMOS Open Drain. 2.5V tolerant.
HVCMOS	High Voltage CMOS buffers. 2.5V tolerant.
HVIN	High Voltage CMOS input-only buffers 3.3V tolerant
SSTL-2	Stub Series Termination Logic. These are 2.6V output capable buffers, 2.6V tolerant.
SSTL-1.8	Stub Series Termination Logic. These are 1.8V output capable buffers, 1.8V tolerant.
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.

2.1 Host Interface Signals

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (Vtt).

Signal Name	Type	Description
HADS#	I/O GTL+	**Address Strobe:** The processor bus owner asserts HADS# to indicate the first of two cycles of a request phase. The MCH can assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O GTL+	**Block Next Request:** Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
HBPRI#	O GTL+	**Priority Agent Bus Request:** The MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O GTL+	**Bus Request 0:** The MCH pulls the processor's bus HBREQ0# signal low during HCPURST#. The processor samples this signal on the active-to-inactive transition of HCPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. HBREQ0# should be tristated after the hold time requirement has been satisfied.
HCPURST#	O GTL+	**Processor Reset:** The HCPURST# pin is an output from the MCH. The MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is deasserted. The HCPURST# allows the processors to begin execution in a known state. **NOTE:** The ICH must provide the processor frequency select strap set-up and hold times around HCPURST#. This requires strict synchronization between MCH HCPURST# deassertion and the ICH driving the straps.
HDBSY#	I/O GTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O GTL+	**Defer:** Signals that the MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
HDINV[3:0]#	I/O GTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0] signals**.** Indicates if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **HDINV[x]# Data Bits** DINV[3]# HD[63:48] DINV[2]# HD[47:32] DINV[1]# HD[31:16] DINV[0]# HD[15:0]
HDRDY#	I/O GTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HEDRDY#	O GTL+	**Early Data Ready:** Indicates that data will be returning on the bus exactly two clocks after assertion.
HA[31:3]#	I/O GTL+	**Host Address Bus:** HA[31:3]# connect to the processor address bus. During processor cycles the HA[31:3]# are inputs. The MCH drives HA[31:3]# during snoop cycles on behalf of DMI and PCI Express* initiators. HA[31:3]# are transferred at 2x rate.
HADSTB[1:0]#	I/O GTL+	**Host Address Strobe:** The source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0] at the 2x transfer rate.

Signal Name	Type	Description
HD[63:0]	I/O GTL+	**Host Data:** These signals are connected to the processor data bus. Data on HD[63:0] is transferred at 4x rate. Note that the data signals may be inverted on the processor bus, depending on the HDINV[3:0]# signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O GTL+	**Differential Host Data Strobes:** The differential source synchronous strobes used to transfer HD[63:0]# and HDINV[3:0]# at 4x transfer rate. Named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence, they are pseudo-differential, and not true differential. **StrobesData Bits** HDSTBP[3#,HD[63:48]DINV[3]# HDSTBN[3]# HDSTBP[2]#,HD[47:32]DINV[2]# HDSTBN[2]# HDSTBP[1]#,HD[31:16]DINV[1]# HDSTBN[1]# HDSTBP[0]#,HD[15:0]DINV[0]# HDSTBN[0]#
HHIT#	I/O GTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HHITM# by the target to extend the snoop window.
HHITM#	I/O GTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HHIT# to extend the snoop window.
HLOCK#	I/O GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic, i.e. no DMI or PCI Express* accesses to DRAM are allowed when HLOCK# is asserted by the processor.
HPCREQ#	I GTL+ 2x	**Precharge Request:** The processor provides a “hint” to the MCH that it is OK to close the DRAM page of the memory read request with which the hint is associated. The MCH uses this information to schedule the read request to memory using the special “AutoPrecharge” attribute. This causes the DRAM to immediately close (Precharge) the page after the read data has been returned. This allows subsequent processor requests to more quickly access information on other DRAM pages, since it will no longer be necessary to close an open page prior to opening the proper page. Asserted by the requesting agent during both halves of Request Phase. The same information is provided in both halves of the request phase.
HREQ[4:0]#	I/O GTL+ 2x	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
HTRDY#	O GTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O GTL+	**Response Signals:** Indicates type of response according to the table below: 000Response type 001Idle state 010Retry response 011Deferred response 100Reserved (not driven by MCH) 101Hard Failure (not driven by MCH) 110No data response 111Implicit Writeback 111Normal data response
BSEL[2:0]	I CMOS	**Bus Speed Select:** At the deassertion of RSTINB, the value sampled on these pins determines the expected frequency of the bus.

Signal Name	Type	Description
HRCOMP	I/O CMOS	**Host RCOMP:** Used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (Vtt). Connects to HXRCOMP1IN in the package.
HSCOMP	I/O CMOS	**Slew Rate Compensation:** Compensation for the Host Interface
HSWING	I A	**Host Voltage Swing:** This signal provides the reference voltage used by FSB RCOMP circuits. HSWING is used for the signals handled by HRCOMP.
HVREF	I A	**Host Reference Voltage Reference:** Voltage input for the Data, Address, and Common clock signals of the Host GTL interface.

2.2 DDR/DDR2 DRAM Channel A Interface

Signal Name	Type	Description
SCLK_A[5:0]	O SSTL-2/1.8	**SDRAM Differential Clock:** (3 per DIMM).) SCLK_A and its complement SCLK_A# signal make a differential clock pair output. The crossing of the positive edge of SCLK_A and the negative edge of its complement SCLK_A# are used to sample the command and control signals on the SDRAM.
SCLK_A[5:0]#	O SSTL-2/1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM) These are the complementary Differential DDR/DDR2 Clock signals.
SCS_A[3:0]#	O SSTL-2/1.8	**Chip Select:** (1 per Rank) These signals select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
SMA_A[13:0]	O SSTL-2/1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM
SBS_A[2:0]	O SSTL-2/1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank DDR: 1Gb technology is 4 banks. SBS_A[2] is not used. DDR2: 1Gb technology is 8 banks.
SRAS_A#	O SSTL-2/1.8	**Row Address Strobe:** Used with SCAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SCAS_A#	O SSTL-2/1.8	**Column Address Strobe:** Used with SRAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SWE_A#	O SSTL-2/1.8	**Write Enable:** Used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the SDRAM commands.
SDQ_A[63:0]	I/O SSTL-2/1.8 2x	**Data Lines:** SDQ_A signals interface to the SDRAM data bus.
SDM_A[7:0]	O SSTL-2/1.8 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_A bit for every data byte lane.
SCB_A[7:0]	I/O SSTL-2/1.8 2x	**ECC Check Byte:** These signals require a 6 layer board to be routed.
SDQS_A[8:0]	I/O SSTL-2/1.8 2x	**Data Strobes:** For DDR the rising and falling edges of SDQS_A are used for capturing data during read and write transactions. For DDR2, SDQS_A and its complement SDQS_A# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_A and its complement SDQS_A# during read and write transactions.

Signal Name	Type	Description
SDQS_A[8:0]#	I/O SSTL-1.8 2x	**Data Strobe Complements (DDR2 only):** These are the complementary DDR2 strobe signals.
SCKE_A[3:0]	O SSTL-2/1.8	**Clock Enable:** (1 per Rank) SACKE is used to initialize the SDRAMs during power-up and to power-down SDRAM ranks.
SODT_A[3:0]	O SSTL-1.8	**On-Die Termination (DDR2 only):** Active On-die Termination Control signals for DDR2 devices.

2.3 DDR/DDR2 DRAM Channel B Interface

Signal Name	Type	Description
SCLK_B[5:0]	O SSTL-2/1.8	**SDRAM Differential Clock:** (3 per DIMM) SCLK_B and its complement SCLK_B# signal make a differential clock pair output. The crossing of the positive edge of SCLK_B and the negative edge of its complement SCLK_B# are used to sample the command and control signals on the SDRAM.
SCLK_B[5:0]#	O SSTL-2/1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM) These are the complementary Differential DDR/DDR2 Clock signals.
SCS_B[3:0]#	O SSTL-2/1.8	**Chip Select:** (1 per Rank) These signals select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank
SMA_B[13:0]	O SSTL-2/1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM
SBS_B[2:0]	O SSTL-2/1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank DDR: 1Gb technology is 4 banks. SBS_B[2] is not used. DDR2: 1Gb technology is 8 banks.
SRAS_B#	O SSTL-2/1.8	**Row Address Strobe:** Used with SCAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands
SCAS_B#	O SSTL-2/1.8	**Column Address Strobe:** Used with SRAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SWE_B#	O SSTL-2/1.8	**Write Enable:** Used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the SDRAM commands.
SDQ_B[63:0]	I/O SSTL-2/1.8 2x	**Data Lines:** SDQ_B signals interface to the SDRAM data bus
SDM_B[7:0]	O SSTL-2/1.8 2x	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SBDM for every data byte lane.
SCB_B[7:0]	I/O SSTL-2/1.8 2x	**ECC Check Byte:** These signals require a 6 layer board to be routed.
SDQS_B[8:0]	I/O SSTL-2/1.8 2x	**Data Strobes:** For DDR the rising and falling edges of SDQS_B are used for capturing data during read and write transactions. For DDR2, SDQS_B and its complement SDQS_B# make up a differential strobe pair. The data is captured at the crossing point of SDQS_B and its complement SDQS_B# during read and write transactions.
SDQS_B[8:0]#	I/O SSTL-1.8 2x	**Data Strobe Complements (DDR2 only):** These are the complementary DDR2 Strobe signals.

Signal Name	Type	Description
SCKE_B[3:0]	O SSTL-2/1.8	**Clock Enable:** (1 per Rank) SCKE_B is used to initialize the SDRAMs during power-up and to power-down SDRAM ranks.
SODT_B[3:0]	O SSTL-1.8	**On-Die Termination (DDR2 only):** Active On-die Termination Control signals for DDR2 devices.

2.4 DDR/DDR2 DRAM Reference and Compensation

Signal Name	Type	Description
SRCOMP[1:0]	I/O	**System Memory RCOMP**
SOCOMP[1:0]	I/O A	**DDR2 On-Die DRAM Over Current Detection (OCD) driver compensation (DDR2 only)**
SM_SLEWIN[1:0]	I A	**Buffer Slew Rate Input**
SM_SLEWOUT[1:0]	O A	**Buffer Slew Rate Output**
SMVREF[1:0]	I A	**SDRAM Reference Voltage:** Reference voltage inputs for each DQ, DM, DQS, and DQS# input signals.

2.5 PCI Express Interface Signals

Unless otherwise specified, PCI Express signals are AC coupled, so the only voltage specified is a maximum 1.2V differential swing.

Signal Name	Type	Description
EXP_RXN[7:0] EXP_RXP[7:0]	I PCIE	PCI Express* Receive Differential Pair
EXP_TXN[7:0] EXP_TXP[7:0]	O PCIE	PCI Express Transmit Differential Pair
EXP_COMPO	I A	PCI Express Output Current and Resistance Compensation
EXP_COMPI	I A	PCI Express Input Current Compensation

2.6 Analog Display Signals

Signal Name	Type	Description
CRTRED	O A	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 150 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).
CRTRED#	O A	**REDB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.

CRTGREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 150 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).
CRTGREEN#	O A	**GREENB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
CRTBLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 150ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).
CRTBLUE#	O A	**BLUEB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
CRTIREFSET	O A	**Resistor Set:** Set point resistor for the internal color palette DAC. A 255 ohm 1% resistor is required between CRTIREF and motherboard ground.
CRTHSYNC	O 2.5V CMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”. 2.5V output
CRTVSYNC	O 2.5V CMOS	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable). 2.5V output.
CRTDDCCLK	I/O 2.5V CMOS	Monitor Control Clock
CRTDDCDATA	I/O 2.5V CMOS	Monitor Control Data

2.7 Clocks, Reset, and Misc.

Signal Name	Type	Description
HCLKP HCLKN	I CMOS	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the MCH logic that is in the Host clock domain.
GCLKP GCLKN	I CMOS	**Differential PCI Express* Clock In:** These pins receive a differential 100 MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
DREFCLKN DREFCLKP	I CMOS	Display PLL Differential Clock In
RSTIN#	I HVIN	**Reset In:** When asserted, this signal will asynchronously reset the MCH logic. This signal is connected to the PLTRST# output of the ICH. All PCI Express output signals and DMI output signals will also tri-state compliant to PCI Express Rev 1.0a specification. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3V tolerant.
PWROK	I HVIN	**Power OK:** When asserted, PWROK is an indication to the MCH that core power has been stable for at least 10 µs.
EXTTS#	I HVCMOS	**External Thermal Sensor Input:** This signal may connect to a precision thermal sensor located on or near the DIMMs. If the system temperature reaches a dangerously high value, then this signal can be used to trigger the start of system thermal management. This signal is activated when an increase in temperature causes a voltage to cross some threshold in the sensor.

Signal Name	Type	Description
BSEL[2:0]	I CMOS	Core / Processor System Bus Frequency Select Strap
MTYPE	I CMOS	**Memory Type Select Strap** 0 = DDR2 1 = DDR
ICH_SYNC#	O HVCMOS	Connected to the MCH_SYNCH# of ICH6

2.8 Direct Media Interface (DMI)

EDS Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I DMI	**Direct Media Interface:** Receive differential pair (Rx)
DMI_TXP[3:0] DMI_TXN[3:0]	O DMI	**Direct Media Interface:** Transmit differential pair (Tx)

2.9 Power and Ground

Name	Voltage	Description
VCC	1.5V	Core Power
VTT	1.2V	Processor System Bus Power
VCC_EXP	1.5V	PCI Express* and DMI Power
VCCSM	1.8V / 2.6V	**System Memory Power:** DDR2: 1.8V DDR: 2.6V
VCC2	2.5V	2.5V CMOS Power
VCCA_EXPPLL	1.5V	PCI Express PLL Analog Power
VCCA_HPLL	1.5V	Host PLL Analog Power
VCCA_SMPLL	1.5V	System Memory PLL Analog Power
VCCA_PDLLA	1.5V	Digital PLLA Analog
VCCA_PDLLB	1.5V	Digital PLLB Analog
VCCA_DAC	2.5V	Display DAC Analog Power
VSSA_DAC	0V	Ground
VSS	0V	Ground

2.10 Reset States and Pull-Ups/Pull-Downs

This section describes the expected states of the MCH I/O buffers during and immediately after the assertion of RSTIN#. The table only refers to the contributions on the interface from the MCH and **does not** reflect any external influence (such as external pull-up/pull-down resistors or external drivers).

Legend:

DRIVE:	Strong drive (to normal value supplied by core logic if not otherwise stated)
TERM:	Normal termination devices are turned on
LV:	Low voltage
HV:	High voltage
IN:	Input buffer enabled
ISO:	Isolate input buffer so that it doesn't oscillate if input left floating
TRI:	Tri-state
PU:	Weak internal pull-up
PD:	Weak internal pull-down
STRAP:	Strap input sampled during assertion or on the deasserting edge of RSTIN#

Interface	Signal Name	I/O	State during RSTIN# Assertion	State after RSTIN# Deassertion	Pull-Up / Pull-Down
HOST	HCPURST#	O	DRIVE LV	TERM HV after approximately 1ms	
	HADSTB[1:0]#	I/O	TERM HV	TERM HV	
	HA[31:3]#	I/O	TERM HV	TERM HV	
	HD[63:0]	I/O	TERM HV	TERM HV	
	HDSTBP[3:0]#	I/O	TERM HV	TERM HV	
	HDSTBN[3:0]#	I/O	TERM HV	TERM HV	
	HDINV[3:0]#	I/O	TERM HV	TERM HV	
	HADS#	I/O	TERM HV	TERM HV	
	HBNR#	I/O	TERM HV	TERM HV	
	HBPRI#	O	TERM HV	TERM HV	
	HDBSY#	I/O	TERM HV	TERM HV	
	HDEFER#	O	TERM HV	TERM HV	
	HDRDY#	I/O	TERM HV	TERM HV	
	HEDRDY#	O	TERM HV	TERM HV	
	HHIT#	I/O	TERM HV	TERM HV	
	HHITM#	I/O	TERM HV	TERM HV	
	HLOCK#	I/O	TERM HV	TERM HV	
	HREQ[4:0]#	I/O	TERM HV	TERM HV	
	HTRDY#	O	TERM HV	TERM HV	
	HRS[2:0]#	O	TERM HV	TERM HV	

Interface	Signal Name	I/O	State during RSTIN# Assertion	State after RSTIN# Deassertion	Pull-Up / Pull-Down
HOST (cont'd)	HBREQ0#	I/O	TERM HV	TERM HV	
	HPCREQ#	I	TERM HV	TERM HV	
	HVREF	I	IN	IN	
	HRCOMP	I/O	TRI	TRI after RCOMP	20 ohm resistor for board with target impedance of 60 ohm
	HSWING	I	IN	IN	
	HSCOMP	I/O	TRI	TRI	
SYSTEM MEMORY	SCLK_A[5:0]	O	TRI	TRI	
	SCLK_A[5:0]#	O	TRI	TRI	
	SCS_A[3:0]#	O	TRI	TRI	
	SMA_A[13:0]	O	TRI	TRI	
	SBS_A[2:0]	O	TRI	TRI	
	SRAS_A#	O	TRI	TRI	
	SCAS_A#	O	TRI	TRI	
	SWE_A#	O	TRI	TRI	
	SDQ_A[63:0]	I/O	TRI	TRI	
	SDM_A[7:0]	O	TRI	TRI	
	SDQS_A[8:0]	I/O	TRI	TRI	
	SDQS_A[8:0]#	I/O	TRI	TRI	
	SCKE_A[3:0]	O	LV	LV	
	SODT_A[3:0]	O	LV	LV	
	SCLK_B[5:0]	O	TRI	TRI	
	SCLK_B[5:0]#	O	TRI	TRI	
	SCS_B[3:0]#	O	TRI	TRI	
	SMA_B[13:0]	O	TRI	TRI	
	SBS_B[2:0]	O	TRI	TRI	
	SRAS_B#	O	TRI	TRI	
	SCAS_B#	O	TRI	TRI	
	SWE_B#	O	TRI	TRI	
	SDQ_B[63:0]	I/O	TRI	TRI	
	SDM_B[7:0]	O	TRI	TRI	
	SDQS_B[8:0]	I/O	TRI	TRI	
	SDQS_B[8:0]#	I/O	TRI	TRI	
	SCKE_B[3:0]	O	LV	LV	
	SODT_B[3:0]	O	LV	LV	
	SRCOMP0	I/O	TRI	TRI after RCOMP	
	SRCOMP1	I/O	TRI	TRI after RCOMP	
	SM_SLEWIN[1:0]	I	IN	IN	

Interface	Signal Name	I/O	State during RSTIN# Assertion	State after RSTIN# Deassertion	Pull-Up / Pull-Down
SYSTEM MEMORY (cont'd)	SM_SLEWOU[1:0]	O	TRI	TRI after RCOMP	
	SMREF[1:0]	I	IN	IN	
	SOCOMP[1:0]	I/O	TRI	TRI	DDR2: 40 ohm resistor to ground
	EXP_RXN[7:0]	I	TRI	TRI	
	EXP_RXP[7:0]	I	TRI	TRI	
	EXP_TXN[7:0]	O	PU	PU	
	EXP_TXP[7:0]	O	PU	PU	
	EXPACOMPO	I	TRI	TRI	
	EXPACOMPI	I	TRI	TRI	
DMI	DMI_RXN[3:0]	I	TRI	TRI	
	DMI_RXP[3:0]	I	TRI	TRI	
	DMI_TXN[3:0]	O	PU	PU	
	DMI_TXP[3:0]	O	PU	PU	
CLOCKS	HCLKN	I	IN	IN	
	HCLKP	I	IN	IN	
	GCLKN	I	IN	IN	
	GCLKP	I	IN	IN	
	DREFCLKN	I	IN	IN	
	DREFCLKP	I	IN	IN	
MISC	RSTIN#	I	IN	IN	
	PWROK	I	HV	HV	
	EXTTS#	I	IN	IN	
	BSEL[2:0]	I	TRI	TRI	
	MTYPE	I	TERM HV	TERM HV	
	EXP_SLR	I	TERM HV	TERM HV	
DAC	CRTHSYNC	O	DRIVE HV	DRIVE TO ARBITRARY VALUE	
	CRTVSYNC	O	DRIVE HV	DRIVE TO ARBITRARY VALUE	
	CRTRED	O	TRI	TRI	
	CRTRED#	O	TRI	TRI	
	CRTGREEN	O	TRI	TRI	
	CRTGREEN#	O	TRI	TRI	
	CRTBLUE	O	TRI	TRI	
	CRTBLUE#	O	TRI	TRI	
	CRTREFSET	O	TRI	0.5 • Bandgap	255 ohm ±1% resistor to ground
	CRTDDCCLK	I/O	TRI	TRI	PU
	CRTDDCDATA	I/O	ITRI	TRI	PU

§

3 Register Description

The MCH contains two sets of software accessible registers, accessed via the processor I/O address space: Control registers and internal configuration registers.

- Control registers are I/O mapped into the processor I/O space that control access to PCI and PCI Express configuration space (see Section 3.4).
- Internal configuration registers residing within the MCH are partitioned into three logical device register sets ("logical" since they reside within a single physical device). The first register set is dedicated to Host Bridge functionality (i.e. DRAM configuration, other chip-set operating parameters and optional features). The second register block is dedicated to Host-PCI Express Bridge functions (controls PCI Express interface configurations and operating parameters). The third register set is dedicated to internal graphics functions.

The MCH internal registers (I/O Mapped, Configuration and PCI Express Extended Configuration registers) are accessible by the processor. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFIG_ADDRESS that can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). Registers that reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in DWord (32-bit) quantities.

3.1 Register Terminology

The following table shows the register-related terminology that is used in this document.

Register Type	Description
RO	Read Only bit(s). Writes to these bits have no effect.
RS/WC	Read Set / Write Clear bit(s). These bits are set to '1' when read and then will continue to remain set until written. A write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect.
R/W	Read / Write bit(s). These bits can be read and written.
R/WC	Read / Write Clear bit(s). These bits can be read. Internal events may set this bit. A write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect.
R/WC/S	Read / Write Clear / Sticky bit(s). These bits can be read. Internal events may set this bit. A write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express* related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec).
R/W/L	Read / Write / Lockable bit(s). These bits can be read and written. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/S	Read / Write / Sticky bit(s). These bits can be read and written. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec.
R/WSC	Read / Write Self Clear bit(s). These bits can be read and written. When the bit is '1', hardware may clear the bit to '0', based upon internal events, possibly sooner than any subsequent read could retrieve a '1'.

Register Type	Description
R/WSC/L	Read / Write Self Clear / Lockable bit(s). These bits can be read and written. When the bit is ‘1’, hardware may clear the bit to ‘0’, based upon internal events, possibly sooner than any subsequent read could retrieve a ‘1’. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
RWC	Read Write Clear bit(s). These bits can be read and written. However, a write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect.
R/WO	Write Once bit(s). Once written, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	Write Only. Whose bits may be written, but will always-return zeros when read. They are used for write side effects. Any data written to these registers cannot be retrieved.
Reserved Bits	Some of the MCH registers described in this section contain reserved bits. These bits are labeled “Reserved”. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the configuration address register.
Reserved Registers	In addition to reserved bits within a register, the MCH contains address locations in the configuration space of the Host Bridge entity that are marked either “Reserved” or “Intel Reserved”. The MCH responds to accesses to “Reserved” address locations by completing the host cycle. When a “Reserved” register location is read, a zero value is returned. (“Reserved” registers can be 8-, 16-, or 32-bits in size). Writes to “Reserved” registers have no effect on the MCH. Registers that are marked as “Intel Reserved” must not be modified by system software. Writes to “Intel Reserved” registers may cause system failure. Reads from “Intel Reserved” registers may return a non-zero value.
Default Value	Upon a Full Reset, the MCH sets its entire set of internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the MCH registers accordingly.

3.2 Platform Configuration Structure

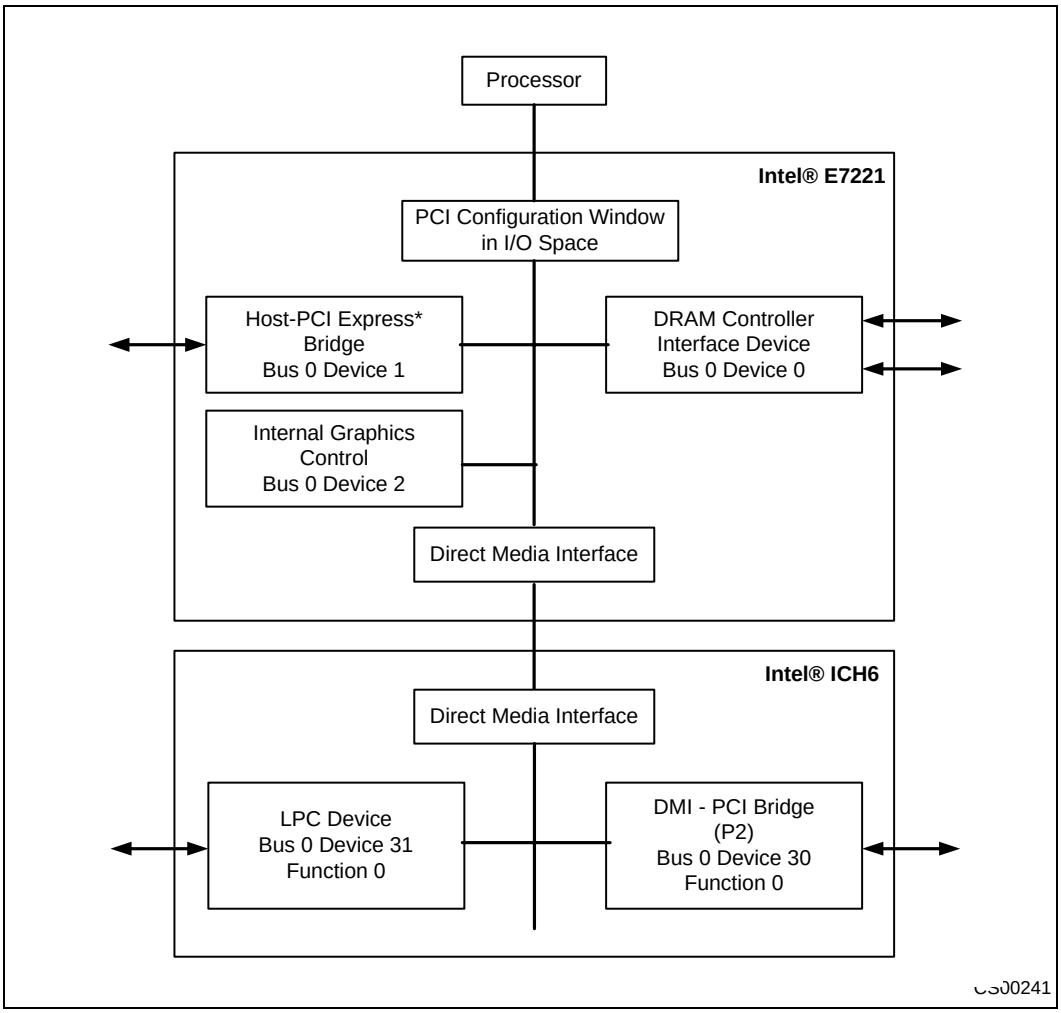
In platforms that support DMI (e.g. this MCH) the configuration structure is significantly different from previous Hub architectures. The DMI physically connects the MCH and the ICH6; so, from a configuration standpoint, the DMI is logically PCI Bus 0. As a result, all devices internal to the MCH and the ICH6 appear to be on PCI Bus 0.

The ICH6 internal LAN controller does not appear on bus 0; it appears on the external PCI bus (whose number is configurable).

The system’s primary PCI expansion bus is physically attached to the ICH6 and, from a configuration perspective, appears to be a hierarchical PCI Bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. The PCI Express appears to system software to be a real PCI Bus behind a PCI-to-PCI bridge that is a device resident on PCI Bus 0.

Note: That a physical PCI Bus 0 does not exist and that DMI and the internal devices in the MCH and ICH6 logically constitute PCI Bus 0 to configuration software. This is shown in Figure 3-1.

Figure 3-1. Conceptual Intel® E7221 Platform PCI Configuration Diagram



The MCH contains three PCI devices within a single physical component. The configuration registers for the three devices are mapped as devices residing on PCI Bus 0.

- **Device 0 – Host Bridge/DRAM Controller:** Logically this appears as a PCI device residing on PCI Bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), and configuration for the DMI and other MCH specific registers.
- **Device 1 – Host-PCI Express Bridge:** Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI Bus 0 and is compliant with *PCI Express Specification*, Revision 1.0a. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.
- **Device 2 – Internal Graphics Control:** Logically, this appears as a PCI device residing on PCI Bus 0. Physically, Device 2 contains the configuration registers for display functions.

3.3 General Routing Configuration Accesses

The MCH supports two PCI related interfaces: DMI and PCI Express. PCI and PCI Express configuration cycles are selectively routed to one of these interfaces. The MCH is responsible for routing configuration cycles to the proper interface. Configuration cycles to the ICH6 internal devices and Primary PCI (including downstream devices) are routed to the ICH6 via DMI.

A detailed description of the mechanism for translating processor I/O bus cycles to configuration cycles is described below.

3.3.1 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based “configuration space” that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the MCH.

The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DW I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI Bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG_ADDRESS [31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The MCH is responsible for translating and routing the processor’s I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal MCH configuration registers, DMI or PCI Express.

3.3.2 Logical PCI Bus 0 Configuration Mechanism

The MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device. The Host-DMI Bridge entity within the MCH is hardwired as Device 0 on PCI Bus 0. The Host-PCI Express Bridge entity within the MCH is hardwired as Device 1 on PCI Bus 0. Device 2 contains the control registers for the Integrated Graphics Controller. The ICH6 decodes the Type 0 access and generates a configuration access to the selected internal device.

3.3.3 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, and falls outside the range claimed by the Host-PCI Express bridge (not between lower bound in device’s SUBORDINATE BUS NUMBER register and lower bound in device’s SECONDARY BUS NUMBER register), the MCH would generate a Type 1 DMI Configuration Cycle. This DMI configuration cycle will be sent over the DMI.

If the cycle is forwarded to the ICH6 via the DMI, the ICH6 compares the non-zero Bus Number with the SECONDARY BUS NUMBER and SUBORDINATE BUS NUMBER registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, one of the ICH's devices, the DMI, or a downstream PCI Bus.

Figure 3-2. DMI Type 0 Configuration Address Translation

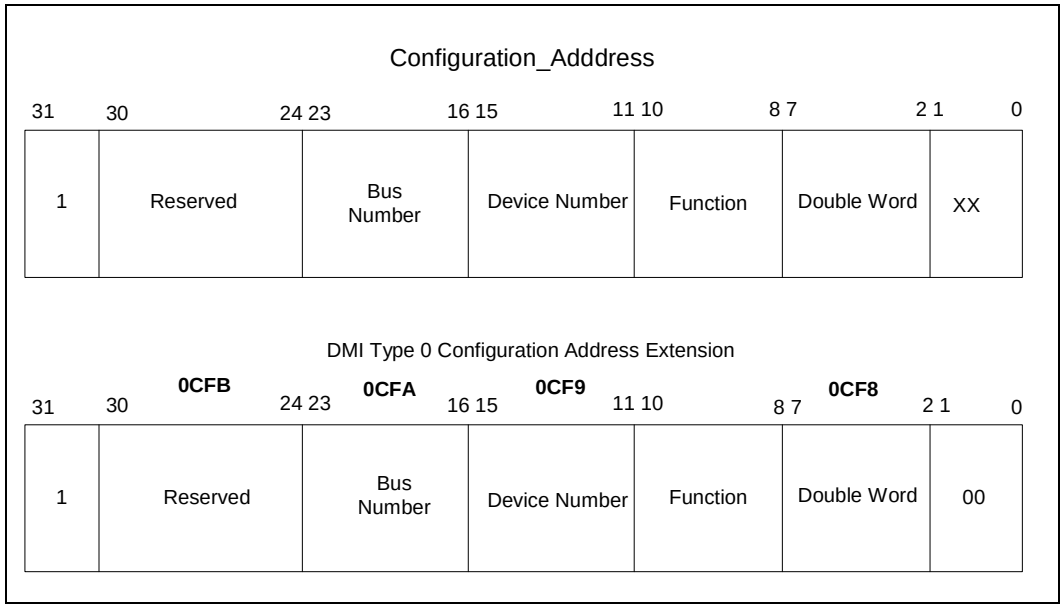
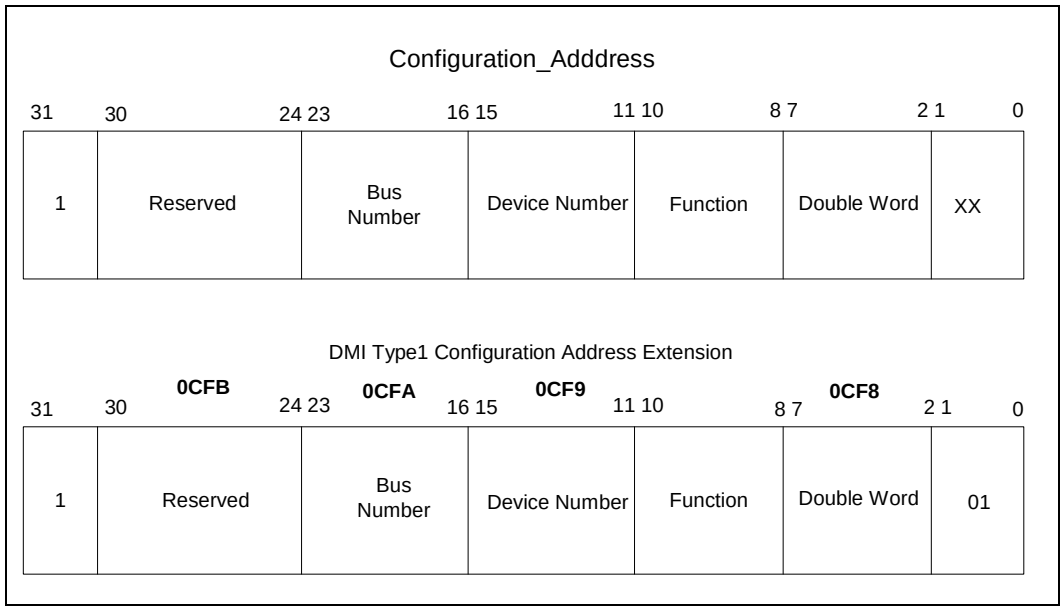


Figure 3-3. DMI Type 1 Configuration Address Translation

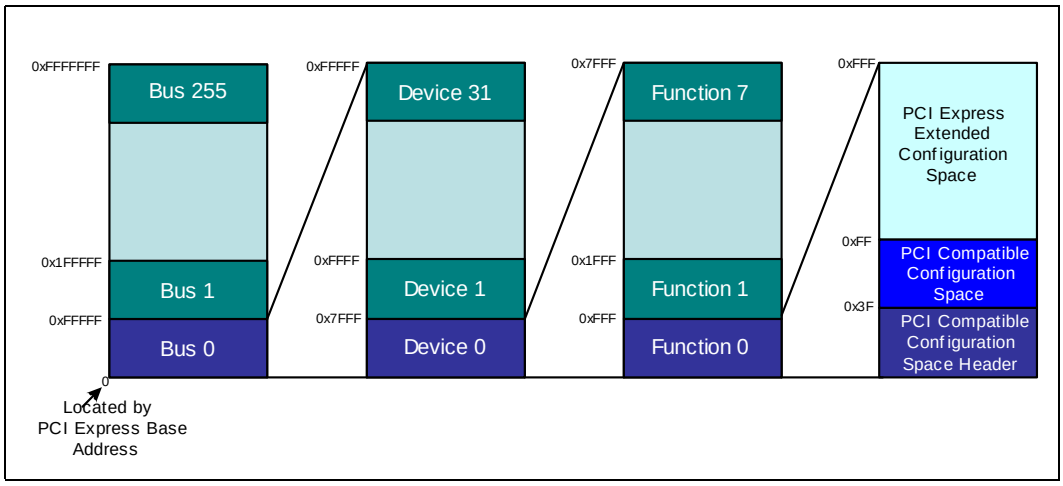


3.3.4 PCI Express Enhanced Configuration Mechanism

PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by the *PCI Specification*, Rev 2.3. PCI Express configuration space is divided into a PCI 2.3 compatible region, which consists of the first 256 bytes of a logical device's configuration space and a PCI Express extended region, which consists of the remaining configuration space.

The PCI compatible region can be accessed using either the mechanism defined in the previous section or using the enhanced PCI Express configuration access mechanism described in this section. The extended configuration registers may only be accessed using the enhanced PCI Express configuration access mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the DWord to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent. The enhanced PCI Express configuration access mechanism utilizes a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. There is a register, PCIEXBAR, that defines the base address for the 256 MB block of addresses below top of addressable memory (currently 4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. The PCI Express Configuration Transaction Header includes an additional 4 bits (Extended Register Address[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all 0's.

Figure 3-4. Memory Map to PCI Express* Device Configuration Space

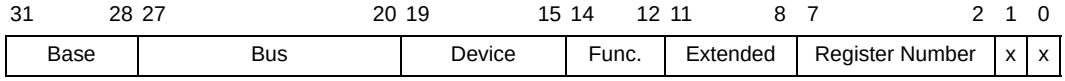


Just the same as with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

To access this space (steps 1, 2, and 3 are done only once by BIOS):

1. Use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 31 of the DEVEN register.
2. Use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register.

3. Calculate the host address of the register you wish to set using (PCI Express base + (bus number • 1 MB) + (device number • 32 KB) + (function number • 4 KB) + (1 B • offset within the function) = host address).
4. Use a memory write or memory read cycle to the calculated host address to write to or read from that register.

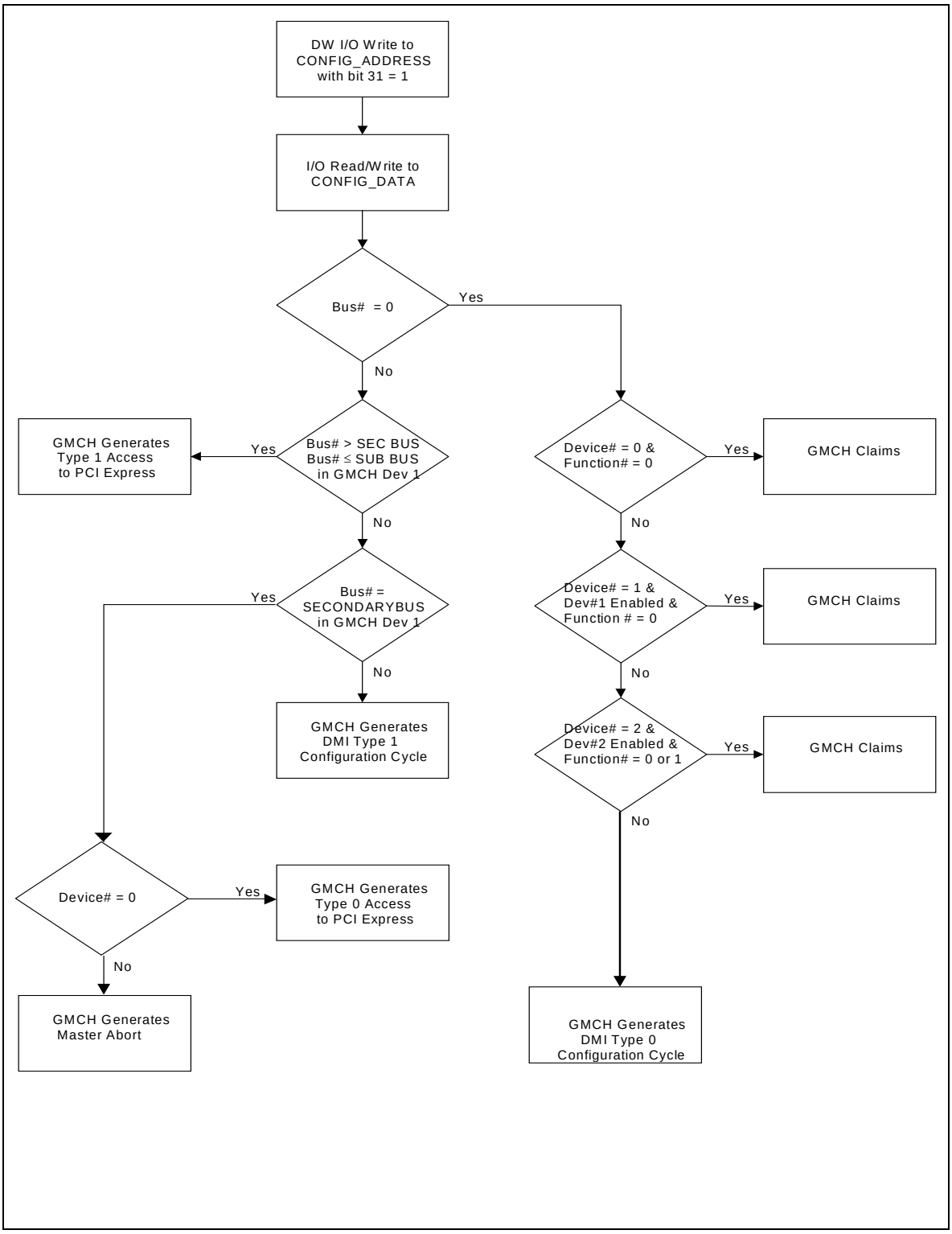


PCI Express Configuration Writes:

- Internally the host interface unit will translate writes to PCI Express extended configuration space to configurations on the backbone.
- The host interface unit will treat the posted write as a non-posted write internal to the host interface unit.
- Writes to extended space are posted on the FSB, but non-posted on the PCI Express (Intel® 6702PXH 64-bit PCI Hub) or DMI pins (i.e. translated to config writes).
- See the PCI Express specification for more information on both the PCI 2.3 compatible and PCI Express enhanced configuration mechanism and transaction rules.

3.3.5 Intel® E7221 MCH Configuration Cycle Flowchart

Figure 3-5. Intel® E7221 MCH Configuration Cycle Flowchart



3.4 I/O Mapped Registers

The MCH contains two registers that reside in the processor I/O address space – the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.4.1 CONFIG_ADDRESS – Configuration Address Register

I/O Address: 0CF8h Accessed as a DW
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DW. A Byte or Word reference will "pass through" the Configuration Address Register and DMI onto the Primary PCI Bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access & Default	Description
31	R/W 0b	**Configuration Enable (CFGE):** When this bit is set to 1, accesses to PCI configuration space are enabled. If this bit is reset to 0, accesses to PCI configuration space are disabled.
30:24		Reserved
23:16	R/W 00h	**Bus Number:** If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus 0 agent. If this is the case and the MCH is not the target (i.e. the device number is >= 3 and not equal to 7), then a DMI Type 0 Configuration Cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by Device 1's SECONDARY BUS NUMBER or SUBORDINATE BUS NUMBER Register, then a DMI Type 1 Configuration Cycle is generated. If the Bus Number is non-zero and matches the value programmed into the SECONDARY BUS NUMBER Register of Device 1, a Type 0 PCI configuration cycle will be generated on PCI Express. If the Bus Number is non-zero, greater than the value in the SECONDARY BUS NUMBER register of Device 1 and less than or equal to the value programmed into the SUBORDINATE BUS NUMBER Register of Device 1 a Type 1 PCI configuration cycle will be generated on PCI Express. This field is mapped to byte 8 [7:0] of the request header format during PCI Express* Configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.
15:11	R/W 00h	**Device Number:** This field selects one agent on the PCI Bus selected by the Bus Number. When the Bus Number field is "00" the MCH decodes the Device Number field. The MCH is always Device Number 0 for the Host bridge entity, Device Number 1 for the Host-PCI Express entity. Therefore, when the Bus Number =0 and the Device Number equals 0,1or 2 the internal MCH devices are selected. This field is mapped to byte 6 [7:3] of the request header format during PCI Express Configuration cycles and A [15:11] during the DMI configuration cycles.
10:8	R/W 000b	**Function Number:** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express Configuration cycles and A[10:8] during the DMI configuration cycles.

Bit	Access & Default	Description
7:2	R/W 00h	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to byte 7 [7:2] of the request header format during PCI Express Configuration cycles and A[7:2] during the DMI Configuration cycles.
1:0		Reserved

3.4.2 CONFIG_DATA – Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access & Default	Description
31:0	R/W 0000 0000h	**Configuration Data Window (CDW):** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

§

4 Host Bridge/DRAM Controller Registers (D0:F0)

The DRAM Controller registers are in Device 0 (D0), Function 0 (F0).

Warning: Address locations that are not listed are considered Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

All registers that are defined in the PCI 2.3 specification, but are not necessary or implemented in this component are simply not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

Table 4-1. Host Bridge Register Address Map (D0:F0) (Sheet 1 of 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
00-01h	VID	Vendor Identification	8086h	RO
02-03h	DID	Device Identification	2588h	RO
04-05h	PCICMD	PCI Command	0006h	RO, R/W
06-07h	PCISTS	PCI Status	0090h	RO, R/W/C
08h	RID	Revision Identification	00h	RO
09-0Bh	CC	Class Code	00h	RO
0Ch	—	Reserved	—	—
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0F-2Bh	—	Reserved	—	—
2C-2Dh	SVID	Subsystem Vendor Identification	0000h	R/W/O
2E-2Fh	SID	Subsystem Identification	0000h	R/W/O
30-33h	—	Reserved	—	—
34h	CAPPTR	Capabilities Pointer	EOh	RO
35-3Fh	—	Reserved	—	—
40-43h	EPBAR	Egress Port Base Address	00000000h	RO
44-47h	MCHBAR	MCH Memory Mapped Register Range Base Address	00000000h	R/W
48-4Bh	PCIEXBAR	PCI Express* Register Range Base Address	E0000000h	R/W
4C-4Fh	DMIBAR	Root Complex Register Range Base Address	00000000h	R/W
50-51h	—	Reserved	—	—
52-53h	GGC	MCH Graphics Control Register	0030h	R/W/L
54-57h	DEVEN	Device Enable	00000019h	R/W
58-5Bh	DEAP	DRAM Error Address Pointer	00000000h	R/W
5Ch	DERRSYN	DRAM Error Syndrome	00h	RO/S
5Dh	DERRDST	DRAM Error Destination	00h	RO/S

Table 4-1. Host Bridge Register Address Map (D0:F0) (Sheet 2 of 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
5E-8Fh	—	Reserved	—	—
90h	PAM0	Programmable Attribute Map 0	00h	R/W
91h	PAM1	Programmable Attribute Map 1	00h	R/W
92h	PAM2	Programmable Attribute Map 2	00h	R/W
93h	PAM3	Programmable Attribute Map 3	00h	R/W
94h	PAM4	Programmable Attribute Map 4	00h	R/W
95h	PAM5	Programmable Attribute Map 5	00h	R/W
96h	PAM6	Programmable Attribute Map 6	00h	R/W
97h	LAC	Legacy Access Control	00h	R/W
98-9Bh	—	Reserved	—	—
9Ch	TOLUD	Top of Low Usable DRAM	08h	R/W
9Dh	SMRAM	System Management RAM Control	00h	RO, R/W/L
9Eh	ESMRAMC	Extended System Management RAM Control	00h	RO, R/W/L
9F-C7h	—	Reserved	—	—
C8-C9h	ERRSTS	Error Status	0000h	RO, R/W/L
CA-CBh	ERRCMD	Error Command	0000h	R/W
CC-CDh	SMICMD	SMI Command	0000h	R/W
CE-CFh	SCICMD	SCI Command	0000h	R/W
D0-DBh	—	Reserved	—	—
DC-DFh	SKPD	Scratch Pad Data	00000000h	R/W
E0-E8h	CAPID0	Capability Identifier	000000000010 90009h	RO

4.1 Configuration Register Details (D0:F0)

4.1.1 VID – Vendor Identification (D0:F0)

PCI Device: 0
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

4.1.2 DID – Device Identification (D0:F0)

PCI Device: 0
Address Offset: 02h
Default Value: 2588h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2588h	**Device Identification Number (DID):** Identifier assigned to the MCH core/ primary PCI device.

4.1.3 PCICMD – PCI Command (D0:F0)

PCI Device: 0
Address Offset: 04h
Default Value: 0006h
Access: RO, R/W
Size: 16 bits

Since MCH Device 0 does not physically reside on Primary PCI bus, many of the bits are not implemented.

Bit	Access & Default	Description
15:10		Reserved
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back write. Since Device 0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no affect.
8	R/W 0b	**SERR Enable (SERRE):** This bit is a global enable bit for Device 0 SERR messaging. The MCH does not have an SERR signal. The MCH communicates the SERR condition by sending an SERR message over DMI to the ICH6. If this bit is set to a 1, the MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS, and PCISTS registers. If SERRE is clear, then the SERR message is not generated by the MCH for Device 0. **NOTE:** This bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring in that device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO 0b	Address/Data Stepping Enable (ADSTEP): Address/data stepping is not implemented in the MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	RO 0b	**Parity Error Enable (PERRE):** PERRB is not implemented by the MCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP):** The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** The MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.

Bit	Access & Default	Description
3	RO 0b	Reserved
2	RO 1b	**Bus Master Enable (BME):** The MCH is always enabled as a master. This bit is hardwired to a “1”. Writes to this bit position have no effect.
1	RO 1b	**Memory Access Enable (MAE):** The MCH always allows access to main memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	RO 0b	**I/O Access Enable (IOAE):** This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.

4.1.4 PCISTS – PCI Status (D0:F0)

PCI Device: 0
Address Offset: 06h
Default Value: 0090h
Access: RO, R/W/C
Size: 16 bits

This status register reports the occurrence of error events on Device 0’s PCI interface. Since the MCH Device 0 does not physically reside on Primary PCI, many of the bits are not implemented.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	R/W/C 0b	**Signaled System Error (SSE):** This bit is set to 1 when the MCH Device 0 generates an SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS, or ERRSTS registers. Software clears this bit by writing a 1 to it.
13	R/WC 0b	**Received Master Abort Status (RMAS):** This bit is set when the MCH generates a DMI request that receives an Unsupported Request completion packet. Software clears this bit by writing a 1 to it.
12	R/WC 0b	**Received Target Abort Status (RTAS):** This bit is set when the MCH generates a DMI request that receives a Completer Abort completion packet. Software clears this bit by writing a 1 to it.
11	RO 0b	**Signaled Target Abort Status (STAS):** The MCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.
10:9	RO 00b	**DEVSEL Timing (DEVT):** These bits are hardwired to “00”. Writes to these bit positions have no affect. Device 0 does not physically connect to Primary PCI. These bits are set to “00” (fast decode) so that optimum DEVSEL timing for Primary PCI is not limited by the MCH.
8	RO 0b	**Master Data Parity Error Detected (DPD):** PERR signaling and messaging are not implemented by the MCH therefore this bit is hardwired to 0. Writes to this bit position have no effect.
7	RO 1b	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to Primary PCI. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for Primary PCI is not limited by the MCH.
6		Reserved

Bit	Access & Default	Description
5	RO 0b	**66 MHz Capable:** Does not apply to PCI Express. Must be hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability standard register resides.
3:0		Reserved

4.1.5 RID – Revision Identification (D0:F0)

PCI Device: 0
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number of the MCH Device 0. These bits are read only and writes to this register have no effect.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. For the A-0 Stepping, this value is 00h.

4.1.6 CC – Class Code (D0:F0)

PCI Device: 0
Address Offset: 09h
Default Value: 060000h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the MCH. This code has the value 06h, indicating a Bridge device.
15:8	RO 00h	**Sub-Class Code (SUBCC):** This is an 8-bit value that indicates the category of Bridge into which the MCH falls. The code is 00h indicating a Host Bridge.
7:0	RO 00h	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

4.1.7 MLT – Master Latency Timer (D0:F0)

PCI Device: 0
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the MCH is not a PCI master. Therefore this register is not implemented.

Bit	Access & Default	Description
7:0		Reserved

4.1.8 HDR – Header Type (D0:F0)

PCI Device: 0
Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 00h	**PCI Header (HDR):** This field always returns 0 to indicate that the MCH is a single function device with standard header layout. Reads and writes to this location have no effect.

4.1.9 SVID – Subsystem Vendor Identification (D0:F0)

PCI Device: 0
Address Offset: 2Ch
Default Value: 0000h
Access: R/W/O
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

4.1.10 SID – Subsystem Identification (D0:F0)

PCI Device: 0
Address Offset: 2Eh
Default Value: 0000h
Access: R/W/O
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem ID (SUBID)**: This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

4.1.11 CAPPTR – Capabilities Pointer (D0:F0)

PCI Device: 0
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access & Default	Description
7:0	RO E0h	**Pointer to the offset of the first capability ID register block:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

4.1.12 EPBAR – Egress Port Base Address (D0:F0)

PCI Device: 0
Address Offset: 40h
Default Value: 00000000h
Access: RO
Size: 32 bits

This is the base address for the Egress Port MMIO Configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to EPBAREN [Dev 0, offset 54h, bit 27].

Bit	Access & Default	Description
31:12	R/W 00000h	**Egress Port MMIO Base Address:** This field corresponds to bits 31 to 12 of the base address Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within total addressable memory space of 4GB. System Software uses this base address to program the MCH MMIO register set.
11:0		Reserved

4.1.13 MCHBAR – MCH Memory Mapped Register Range Base Address (D0:F0)

PCI Device: 0
Address Offset: 44h
Default Value: 00000000h
Access: R/W
Size: 32 bits

This is the base address for the MCH Memory Mapped Configuration space. There is no physical memory within this 16KB window that can be addressed. The 16KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset 54h, bit 28].

Bit	Access & Default	Description
31:14	R/W 00000h	**MCH Memory Mapped Base Address:** This field corresponds to bits 31 to 14 of the base address MCH Memory Mapped configuration space. BIOS will program this register resulting in a base address for a 16KB block of contiguous memory address space. This register ensures that a naturally aligned 16KB space is allocated within total addressable memory space of 4GB. System Software uses this base address to program the MCH Memory Mapped register set.
13:0		Reserved

4.1.14 PCIEXBAR – PCI Express Register Range Base Address (D0:F0)

PCI Device: 0
Address Offset: 48h
Default Value: E0000000h
Access: R/W
Size: 32 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4KB of configuration space for each PCI Express device that can potentially be part of the PCI Express Hierarchy associated with the MCH. There is not actual physical memory within this 256 MB window that can be addressed. Each PCI Express Hierarchy requires a PCI Express BASE register. The MCH supports one PCI Express hierarchy.

The 256MB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. For example MCHBAR reserves a 16KB space and reserves a 4KB space both outside of PCIEXBAR space. They cannot be overlaid on the space reserved by PCIEXBAR for Device 0.

On reset, this register is disabled and must be enabled by writing a 1 to PCIEXBAREN [Dev 0, offset 54h, bit 31].

If the PCI Express Base Address [bits 31:28] were set to Fh, an overlap with the High BIOS area, APIC ranges would result. Software must guarantee that these ranges do not overlap. The PCI Express Base Address cannot be less than the maximum address written to the Top of physical memory register (TOLUD). If a system is populated with more than 3.5GB, either the PCI Express Enhanced Access mechanism must be disabled or the value in TOLUD must be reduced to report that only 3.5GB are present in the system to allow a value of Eh for the PCI Express Base Address (assuming that all PCI 2.3 compatible configuration space fits above 3.75GB).

Bit	Access & Default	Description
31:28	R/W Eh	**PCI Express* Base Address:** This field corresponds to bits 31 to 28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a 256MB block of contiguous memory address space. Having control of those particular 4-bits insures that this base address will be on a 256MB boundary, above the lowest 256MB and still within total addressable memory space, currently 4GB. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address + Bus Number • 1 MB + Device Number • 32 KB + Function Number • 4 KB The address used to access the PCI Express configuration space for **Device 1** in this component would be PCI Express Base Address + 0 • 1 MB + 1 • 32 KB + 0 • 4 KB = **PCI Express Base Address + 32KB**. Remember that this address is the beginning of the 4KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
27:0		Reserved

4.1.15 DMIBAR – Root Complex Register Range Base Address (D0:F0)

PCI Device: 0
Address Offset: 4Ch
Default Value: 00000000h
Access: R/W
Size: 32 bits

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express Hierarchy associated with the MCH. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to the DMIBAREN [Dev 0, offset 54h, bit 29].

Bit	Access & Default	Description
31:12	R/W 00000h	**DMI Base Address:** This field corresponds to bits 31 to 12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within total addressable memory space of 4GB. System Software uses this base address to program the DMI register set.
11:0		Reserved

4.1.16 GGC – MCH Graphics Control Register (D0:F0)

PCI Device: 0
Address Offset: 52h
Default Value: 0030h
Access: R/W/L
Size: 16 bits

Bit	Access & Default	Descriptions
15:7		**Reserved**
6:4	R/W/L 011b	**Graphics Mode Select (GMS).** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 000: No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. 001: DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010: Reserved 011: DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100: Reserved 101: Reserved 110: Reserved 111: Reserved **NOTE:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

Bit	Access & Default	Descriptions
3:2		Reserved
1	R/W 0b	**IGD VGA Disable (IVD).** 0 = Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1 = Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.
0		Reserved

4.1.17 DEVEN – Device Enable (D0:F0)

PCI Device: 0
Address Offset: 54h
Default Value: 00000019h
Access: R/W
Size: 32 bits

Allows for enabling/disabling of PCI devices and functions that are within the MCH.

The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access & Default	Description
31	R/W 0b	**PCIEXBAR Enable (PCIEXBAREN):** 0 = The PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR bits 31:28 are R/W with no functionality behind them. 1 = The PCIEXBAR register is enabled. Memory read and write transactions whose address bits 31:28 match PCIEXBAR 31:28 will be translated to configuration reads and writes within the MCH. These translated cycles are routed as shown in the table above.
30		**Reserved**
29	R/W 0b	**DMIBAR Enable (DMIBAREN):** 0 = DMIBAR is disabled and does not claim any memory. 1 = DMIBAR memory mapped accesses are claimed and decoded appropriately.
28	R/W 0b	**MCHBAR Enable (MCHBAREN):** 0 = MCHBAR is disabled and does not claim any memory. 1 = MCHBAR memory mapped accesses are claimed and decoded appropriately.
27	R/W 0b	**EPBAR Enable (EPBAREN):** 0 = EPBAR is disabled and does not claim any memory. 1 = EPBAR memory mapped accesses are claimed and decoded appropriately.
26:42		Reserved
3	R/W	**Internal Graphics Engine Function 0 (D2F0EN):** 0 = Bus 0 Device 2 Function 0 is disabled and hidden 1 = Bus 0 Device 2 Function 0 is enabled and visible

Bit	Access & Default	Description
1	R/W 1b Strap-dependent	**PCI Express Port (D1EN):** 0 = Bus 0 Device 1 Function 0 is disabled and hidden. Also gates PCI Express* internal clock and assert PCI Express internal reset. 1 = Bus 0 Device 1 Function 0 is enabled and visible.
0	RO 1b	**Host Bridge:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

4.1.18 DEAP – DRAM Error Address Pointer (D0:F0)

PCI Device: 0
Address Offset: 58h
Default Value: 00000000h
Access: RO/S
Size: 32 bits

This register contains the address of detected DRAM ECC error(s).

Bit	Access & Default	Description
31:7	RO/S 0000000h	**Error Address Pointer (EAP):** This field is used to store the 128B (Two Cache Line) address of main memory for which an error (single bit or multi-bit error) has occurred. Note that the value of this bit field represents the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. A multiple bit error will overwrite a single bit error. Once the error flag bits are set as a result of an error, this bit field is locked and doesn't change as a result of a new error. These bits are reset on PWROK.
6:1		**Reserved**
0	RO/S 0b	**Channel Indicator:** This bit indicates which memory channel had the error. 0 = Channel 0 1 = Channel 1

4.1.19 DERRSYN – DRAM Error Syndrome (D0:F0)

PCI Device: 0
Address Offset: 5Ch
Default Value: 00h
Access: RO/S
Size: 8 bits

This register is used to report the ECC syndromes for each quad word of a 32B-aligned data quantity read from the DRAM array.

Bit	Access & Default	Description
7:0	RO/S 00h	**DRAM ECC Syndrome (DECCSYN):** After a DRAM ECC error on any QW of the data chunk resulting from a read command, hardware loads this field with a syndrome that describes the set of bits associated with the first QW containing an error. Note that this field is locked from the time that it is loaded up to the time when the error flag is cleared by software. If the first error was a single bit, correctable error, then a subsequent multiple bit error on any of the QWs in this read transaction or any subsequent read transaction will cause the field to be rerecorded. When a multiple bit error is recorded, then the field is locked until the error flag is cleared by software. In all other cases, an error, which occurs after the first error, and before the error flag, has been cleared by software, will escape recording. These bits are reset on PWROK.

4.1.20 DERRDST – DRAM Error Destination (D0:F0)

PCI Device: 0
Address Offset: 5Dh
Default Value: 00h
Access: RO/S
Size: 8 bits

This register is used to report the destination of the data containing an ECC error whose address is recorded in DEAP register.

Bit	Access & Default	Description
7:6		Reserved
5:0	RO/S 00h	**Error Source Code:** This field is updated concurrently with DERRSYN. 00h: Processor to memory reads 01h-07h: Reserved 08h-09h: DMI VC0 initiated and targeting cycles/data 0Ah-0Bh: DMI VC1 initiated and targeting cycles/data 0Ch-0Dh: DMI VCp initiated and targeting cycles/data 0Eh-0Fh: Reserved 10h: PCI Express initiated and targeting cycles/data 11h: Reserved 12h: PCI Express initiated and targeting cycles/data 13h: Reserved 14h-16h: PCI Express initiated and targeting cycles/data 17h: Reserved 18h: IGD non-cacheable Async port 19h: IGD non-cacheable Isoch port 1Ah: IGD cacheable port 1Bh-3Eh: Reserved 3Fh: Used for broadcast messages with data targeting multiple units. (e.g. EOI). These bits are reset on PWROK.

4.1.21 PAM0 – Programmable Attribute Map 0 (D0:F0)

PCI Device: 0
Address Offset: 90h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h-0FFFFFh

The MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cache ability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

RE – Read Enable. When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PRIMAY PCI.

WE – Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PRIMAY PCI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 KB in size.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0F0000-0FFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that addresses the BIOS area from 0F0000 to 0FFFFF. 00: DRAM Disabled: All accesses are directed to the DMI. 01: Read Only: All reads are sent to DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0		Reserved

Warning: The MCH may hang if a PCI Express or DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM). For these reasons the following critical restriction is placed on the programming of the PAM regions:

At the time that a DMI or PCI Express accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

4.1.22 PAM1 – Programmable Attribute Map 1 (D0:F0)

PCI Device: 0
Address Offset: 91h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h-0C7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0C4000-0C7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000 to 0C7FFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0C0000-0C3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000 to 0C3FFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.23 PAM2 – Programmable Attribute Map 2 (D0:F0)

PCI Device: 0
Address Offset: 92h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h-0CFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0CC000-0CFFFF Attribute (HIENABLE):** 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

Bit	Access & Default	Description
3:2		Reserved
1:0	R/W 00b	**0C8000-0CBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000 to 0CBFFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.24 PAM3 – Programmable Attribute Map 3 (D0:F0)

PCI Device: 0
Address Offset: 93h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h-0D7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0D4000-0D7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000 to 0D7FFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0D0000-0D3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000 to 0D3FFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.25 PAM4 – Programmable Attribute Map 4 (D0:F0)

PCI Device: 0
Address Offset: 94h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h-0DFFFFh.

Bit	Access & Default	Description
7:6		Reserved

Bit	Access & Default	Description
5:4	R/W 00b	**0DC000-0DFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000 to 0DFFFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0D8000-0DBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000 to 0DBFFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.26 PAM5 – Programmable Attribute Map 5 (D0:F0)

PCI Device: 0
Address Offset: 95h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h-0E7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0E4000-0E7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000 to 0E7FFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0E0000-0E3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000 to 0E3FFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.27 PAM6 – Programmable Attribute Map 6 (D0:F0)

PCI Device: 0
Address Offset: 96h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h-0EFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0EC000-0EFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000 to 0E7FFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0E8000-0EBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000 to 0E3FFF. 00: DRAM Disabled: Accesses are directed to the DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.28 LAC – Legacy Access Control (D0:F0)

PCI Device: 0
Address Offset: 97h
Default Value: 00h
Access: R/W
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15-16 MB.

Bit	Access & Default	Description
7	R/W 0b	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies “behind” this space is not remapped. 0 = No memory hole. 1 = Memory hole from 15 MB to 16 MB.
6:1		Reserved

Bit	Access & Default	Description
0	R/W 0b	**MDA Present (MDAP):** This bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of processor initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if Device 1's VGA Enable bit is not set. If Device 1's VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh are forwarded to the DMI. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to the DMI. MDA resources are defined as the following: Memory: 0B0000h – 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (Including ISA address aliases, A [15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the DMI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: **VGAENMDAPDescription** 0 0 All References to MDA and VGA space are routed to the DMI 0 1 Illegal combination 1 0 All VGA and MDA references are routed to PCI Express* Graphics Attach. 1 1 All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to the DMI

4.1.29 TOLUD – Top of Low Usable DRAM (D0:F0)

PCI Device: 0
Address Offset: 9Ch
Default Value: 08h
Access: R/W
Size: 8 bits

This 8-bit register defines the Top of Low Usable DRAM. TSEG and Graphics Stolen Memory are within the DRAM space defined. From the top, MCH optionally claims 1 to 32MB of DRAM for internal graphics if enabled, and 1, 2, or 8 MB of DRAM for TSEG if enabled.

Bit	Access & Default	Description
7:3	R/W 01h	**Top of Low Usable Dram (TOLUD):** This register contains bits 31 to 27 of an address one byte above the maximum DRAM memory that is usable by the operating system. Address bits 31 down to 27 programmed to 01h implies a minimum memory size of 128 MB. Configuration software must set this value to the smaller of the following two choices: Maximum amount of memory in the system plus one byte or the minimum address allocated for PCI memory. Address bits 26:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. If this register is set to 00000b it implies 128MB's of system memory. **NOTE:** That the Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and Tseg. The host interface determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by 1 MB to determine base of TSEG.

Bit	Access & Default	Description
2:0		Reserved

Programming Example:

C1DRB3 is set to 4GB
TSEG is enabled and TSEG size is set to 1 MB
Internal Graphics is enabled and Graphics Mode Select is set to 32 MB
BIOS knows the OS requires 1G of PCI space
BIOS also knows the range from FEC0_0000h to FFFF_FFFFh is not usable by the system; this 20 MB range at the very top of addressable memory space is lost to APIC.
According to the above equation, TOLUD is originally calculated to:
4GB = 1_0000_0000h

The system memory requirements are:
4GB (max addressable space) – 1GB (PCI space) – 20 MB (lost memory) = 3GB – 128 MB (minimum granularity) = B800_0000h
Since B800_0000h (PCI and other system requirements) is less than 1_0000_0000h; TOLUD should be programmed to B8h.

4.1.30 SMRAM – System Management RAM Control (D0:F0)

PCI Device: 0
Address Offset: 9Dh
Default Value: 00h
Access: R/W/L, RO
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access & Default	Description
7		Reserved
6	R/W/L 0b	**SMM Space Open (D_OPEN):** (When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	R/W/L 0b	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	R/W/L 0b	**SMM Space Locked (D_LCK):** When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.

Bit	Access & Default	Description
3	R/W/L 0b	**Global SMRAM Enable (G_SMRAME):** If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to Section 10.4 for more details. Once D_LCK is set, this bit becomes read only.
2:0	RO 010b	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the MCH supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010.

4.1.31 ESMRAMC – Extended System Management RAM Control (D0:F0)

PCI Device: 0
Address Offset: 9Eh
Default Value: 00h
Access: R/W/L, RO
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Access & Default	Description
7	R/W/L 0b	**Enable High SMRAM (H_SMRAME):** Controls the SMM memory space location (i.e. above 1 MB or below 1 MB) When G_SMRAME is 1 and H_SMRAME this bit is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	R/W/C 0b	**Invalid SMRAM Access (E_SMERR):** This bit is set when the processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO 1b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to "1" by the MCH.
4	RO 1b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to "1" by the MCH.
3	RO 1b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to "1" by the MCH.

Bit	Access & Default	Description
2:1	R/W/L 00b	**TSEG Size (TSEG_SZ):** Selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled. 00: 1 MB TSEG. (TOLUD – Graphics Stolen Memory Size – 1M) to (TOLUD – Graphics Stolen Memory Size). 01: 2 MB TSEG (TOLUD – Graphics Stolen Memory Size – 2M) to (TOLUD – Graphics Stolen Memory Size). 10: 8 MB TSEG (TOLUD – Graphics Stolen Memory Size – 8M) to (TOLUD – Graphics Stolen Memory Size). 11: Reserved. Once D_LCK has been set, these bits become read only.
0	R/W/L 0b	**TSEG Enable (T_EN):** Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

4.1.32 ERRSTS – Error Status (D0:F0)

PCI Device: 0
Address Offset: C8h
Default Value: 0000h
Access: R/WC/S, RO
Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. An SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a “1” to it.

Bit	Access & Default	Description
15:13		Reserved
12	R/WC/S 0b	**MCH Software Generated Event for SMI:** This indicates the source of the SMI was a Device 2 Software Event.
11	R/WC/S 0b	**MCH Thermal Sensor Event for SMI/SCI/SERR:** Indicates that a MCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event.
10		Reserved
9	R/WC/S 0b	**LOCK to non-DRAM Memory Flag (LCKF):** When this bit is set to 1, the MCH has detected a lock operation to memory space that did not map into DRAM.
8	R/WC/S 0b	**Received Refresh Timeout Flag (RRTOF):** This bit is set when 1024 memory core refreshes are enqueued.
7	R/WC/S 0b	**DRAM Throttle Flag (DTF):** 1 = Indicates that a DRAM Throttling condition occurred. 0 = Software has cleared this flag since the most recent throttling event

Bit	Access & Default	Description
6:2		Reserved
1	R/WC/S 0b	**Multiple-bit DRAM ECC Error Flag (DMERR):** If this bit is set to 1, a memory read data transfer had an uncorrectable multiple-bit error. When this bit is set the address, channel number, and device number that caused the error are logged in the EAP register. Once this bit is set the EAP, CN, DN, and ES fields are locked until the processor clears this bit by writing a 1. Software uses bits [1:0] to detect whether the logged error address is for Single or Multiple-bit error. This bit is reset on PWROK.
0	R/WC/S 0b	**Single-bit DRAM ECC Error Flag (DSERR):** If this bit is set to 1, a memory read data transfer had a single-bit correctable error and the corrected data was sent for the access. When this bit is set the address and device number that caused the error are logged in the EAP register. Once this bit is set the EAP, CN, DN, and ES fields are locked to further single bit error updates until the processor clears this bit by writing a 1. A multiple bit error that occurs after this bit is set will overwrite the EAP, CN, and DN fields with the multiple-bit error signature and the MEF bit will also be set. This bit is reset on PWROK.

4.1.33 ERRCMD – Error Command (D0:F0)

PCI Device: 0
Address Offset: CAh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register controls the MCH responses to various system errors. Since the MCH does not have an SERRB signal, SERR messages are passed from the MCH to the ICH6 over DMI. When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Access & Default	Description
15:12		Reserved
11	R/W 0b	**SERR on MCH Thermal Sensor Event (TSESERR)** 1 = The MCH generates a DMI SERR special cycle when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event. 0 = Reporting of this condition via SERR messaging is disabled.
10		Reserved
9	R/W 0b	**SERR on LOCK to non-DRAM Memory (LCKERR)** 1 = The MCH will generate a DMI SERR special cycle whenever a processor lock cycle is detected that does not hit DRAM. 0 = Reporting of this condition via SERR messaging is disabled.
8	R/W 0b	**SERR on DRAM Refresh Timeout (DRTOERR)** 1 = The MCH generates a DMI SERR special cycle when a DRAM Refresh timeout occurs. 0 = Reporting of this condition via SERR messaging is disabled.

Bit	Access & Default	Description
7	R/W 0b	**SERR on DRAM Throttle Condition (DTCERR)** 1 = The MCH generates a DMI SERR special cycle when a DRAM Read or Write Throttle condition occurs. 0 = Reporting of this condition via SERR messaging is disabled.
6:2		Reserved
1	R/W 0b	**SERR Multiple-Bit DRAM ECC Error (DMERR)** 1 = The MCH generates an SERR message over DMI when it detects a multiple-bit error reported by the DRAM controller. 0 = Reporting of this condition via SERR messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	R/W 0b	**SERR on Single-bit ECC Error (DSERR)** 1 = The MCH generates an SERR special cycle over DMI when the DRAM controller detects a single bit error. 0 = Reporting of this condition via SERR messaging is disabled. For systems that do not support ECC this bit must be disabled.

4.1.34 SMICMD – SMI Command

PCI Device: 0
Address Offset: CCh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Bit	Access & Default	Description
15:2		Reserved
1	R/W 0b	**SMI on Multiple-Bit DRAM ECC Error (DMESMI):** 1 = The MCH generates an SMI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0 = Reporting of this condition via SMI messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	R/W 0b	**SMI on Single-bit ECC Error (DSESMI):** 1 = The MCH generates an SMI DMI special cycle when the DRAM controller detects a single bit error. 0 = Reporting of this condition via SMI messaging is disabled. For systems that do not support ECC this bit must be disabled.

4.1.35 SCICMD – SCI Command

PCI Device: 0
Address Offset: CEh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Bit	Access & Default	Description
15:2		Reserved
1	R/W 0b	**SCI on Multiple-Bit DRAM ECC Error (DMESCI):** 1 = The MCH generates an SCI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0 = Reporting of this condition via SCI messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	R/W 0b	**SCI on Single-bit ECC Error (DSESCI):** 1 = The MCH generates an SCI DMI special cycle when the DRAM controller detects a single bit error. 0 = Reporting of this condition via SCI messaging is disabled. For systems that do not support ECC this bit must be disabled.

4.1.36 SKPD – Scratch Pad Data (D0:F0)

PCI Device: 0
Address Offset: DCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access & Default	Description
31:0	R/W 00000000h	**Scratch Pad Data:** 1 DWord of data storage.

4.1.37 CAPID0 – Capability Identifier (D0:F0)

PCI Device: 0
Address Offset: E0h
Default Value: 000000000001090009h
Access: RO
Size: 72 bits

The Capability Identifier Register uniquely identifies Chipset capabilities. This register is Read Only. Writes to this register have no effect.

Bit	Access & Default	Description
71:28		Reserved
27:24	RO 1h	**CAPID Version:** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO 09h	**CAPID Length:** This field has the value 09h to indicate the structure length (9 bytes).
15:8	RO 00h	**Next Capability Pointer:** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09h	**CAP_ID:** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

§

5 MCHBAR Registers

These registers are offset from the MCHBAR base address.

Table 5-1. MCHBAR Register Map (Sheet 1 of 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
100h	C0DRB0	Channel A DRAM Rank Boundary Address 0	00h	R/W
101h	C0DRB1	Channel A DRAM Rank Boundary Address 1	00h	R/W
102h	C0DRB2	Channel A DRAM Rank Boundary Address 2	00h	R/W
103h	C0DRB3	Channel A DRAM Rank Boundary Address 3	00h	R/W
104–107h	—	Reserved	—	—
108h	C0DRA0	Channel A DRAM Rank 0,1 Attribute	00h	R/W
109h	C0DRA2	Channel A DRAM Rank 2,3 Attribute	00h	R/W
10A–10Bh	—	Reserved	—	—
10Ch	C0DCLKDIS	Channel A DRAM Clock Disable	00h	R/W
10Dh	—	Reserved	—	—
10E–10Fh	C0BNKARC	Channel A DRAM Bank Architecture	0000h	R/W
110–113h	—	Reserved	—	—
114–117h	C0DRT1	Channel A DRAM Timing Register	900122h	R/W
118–11Fh	—	Reserved	—	—
120–123h	C0DRC0	Channel A DRAM Controller Mode 0	00000000h	R/W, RO
124–17Fh	—	Reserved	—	—
180h	C1DRB0	Channel B DRAM Rank Boundary Address 0	00h	R/W
181h	C1DRB1	Channel B DRAM Rank Boundary Address 1	00h	R/W
182h	C1DRB2	Channel B DRAM Rank Boundary Address 2	00h	R/W
183h	C1DRB3	Channel B DRAM Rank Boundary Address 3	00h	R/W
184–187h	—	Reserved	—	—
188h	C1DRA0	Channel B DRAM Rank 0,1 Attribute	00h	R/W
189h	C1DRA2	Channel B DRAM Rank 2,3 Attribute	00h	R/W
18A–18B	—	Reserved	—	—
18Ch	C1DCLKDIS	Channel B DRAM Clock Disable	00h	R/W
18Dh	—	Reserved	—	—
18E–18Fh	C1BNKARC	Channel B Bank Architecture	0000h	R/W
190–193h	—	Reserved	—	—
194h	C1DRT1	Channel B DRAM Timing Register 1	900122h	R/W, RO
195–19Fh	—	Reserved	—	—
1A0–1A3h	C1DRC0	Channel B DRAM Controller Mode 0	00000000h	R/W, RO
1A4–F0Fh	—	Reserved	—	—

Table 5-1. MCHBAR Register Map (Sheet 2 of 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
F00h	PMC2C3TT	C2 to C3 Transition Timer	00000000h	R/W
F04h	PMC3C4TT	C3 to C4 Transition Timer	00000000h	R/W
F08h	PMSLFRFC	DRAM Self Refresh Control	0000h	R/W
F10–F13h	PMCFG	Power Management Configuration	00000000h	R/W
F14h	PMSTS	Power Management Status	00000000h	R/W/C/S

5.1 MCHBAR Register Details

5.1.1 C0DRB0 – Channel A DRAM Rank Boundary Address 0

MMIO Range: MCHBAR
Address Offset: 100h
Size: 8 bits

The **DRAM Rank Boundary Register** defines the upper boundary address of each DRAM rank with a granularity of 32 MB. Each rank has its own single-byte **DRB** register. These registers are used to determine which chip select will be active for a given address.

Channel and Rank Map:

Channel A Rank 0: 100h
Channel A Rank 1: 101h
Channel A Rank 2: 102h
Channel A Rank 3: 103h
Channel B Rank 0: 180h
Channel B Rank 1: 181h
Channel B Rank 2: 182h
Channel B Rank 3: 183h

Examples:

1. Single Channel or Asymmetric Channels

   If the channels are independent, addresses in Channel B should begin where addresses in Channel A left off, and the address of the first rank of Channel A can be calculated from the technology (256 Mb, 512 Mb, or 1 Gb) and the x8 or x16 configuration. With independent channels a value of 01h in **C0DRB0** indicates that 32MB of DRAM has been populated in the first rank, and the top address in that rank is 32MB.

   Programming guide:

   If Channel A is empty, all of the C0DRBs are programmed with 00h.

   C0DRB0 = Total memory in chA rank0 (in 32MB increments)

   C0DRB1 = Total memory in chA rank0 + chA rank1 (in 32MB increments)

   ——

   C1DRB0 = Total memory in chA rank0 + chA rank1 + chA rank2 + chA rank3 + chB rank0 (in 32 MB increments)

   If Channel B is empty, all of the C1DRBs are programmed with the same value as C0DRB3.

2. Interleaved Channels or Lockstep

   If channels are interleaved, corresponding ranks in opposing channels will contain the same value, and the value programmed takes into account the fact that twice as many addresses are spanned by this rank compared to the single channel case. With interleaved channels, a value of 01h in **C0DRB0** and a value of 01h in **C1DRB0** indicate that 32MB of DRAM has been populated in the first rank of each channel and the top address in that rank of either channel is 64MB.

   Programming guide:

   C0DRB0 = C1DRB0 = Total memory in chA rank0 (in 32 MB increments)

   C0DRB1 = C1DRB1 = Total memory in chA rank0 + chA rank1 (in 32 MB increments)

   ——

   C0DRB3 = C1DRB3 = Total memory in chA rank0 + chA rank1+ chA rank2 + chA rank3 (in 32 MB increments)

Note: Channel A DRB3 and Channel B CRB3 must be equal for this mode, but the other DRBs may be different.

In all modes, if a DIMM is single sided, it appears as a populated rank and an empty rank. A DRB must be programmed appropriately for each.

Each Rank is represented by a byte. Each byte has the following format.

Bit	Access & Default	Description
7:0	R/W 00h	**Channel A DRAM Rank Boundary Address:** This 8 bit value defines the upper and lower addresses for each DRAM rank. Bits 6:2 are compared against Address 31:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0's. Bit 7 may be programmed to a “1” in the highest DRB (DRB3) if 4GB of memory is present.

5.1.2 C0DRB1 – Channel A DRAM Rank Boundary Address 1

MMIO Range: MCHBAR
Address Offset: 101h
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.3 C0DRB2 – Channel A DRAM Rank Boundary Address 2

MMIO Range: MCHBAR
Address Offset: 102h
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.4 C0DRB3 – Channel A DRAM Rank Boundary Address 3

MMIO Range: MCHBAR
Address Offset: 103h
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.5 C0DRA0 – Channel A DRAM Rank 0,1 Attribute

MMIO Range: MCHBAR
Address Offset: 108h
Size: 8 bits

The **DRAM Rank Attribute Registers** define the page sizes to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the **CxDRA** registers describes the page size of a pair of ranks.

Channel and Rank Map:

Channel A Rank 0, 1: 108h
Channel A Rank 2, 3: 109h
Channel B Rank 0, 1: 188h
Channel B Rank 2, 3: 189h

Bit	Access & Default	Description
7		Reserved
6:4	R/W 000b	**Channel A DRAM odd Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated 001: Reserved 010: 4KB 011: 8KB 100: 16KB Others: Reserved
3		Reserved
2:0	R/W 000b	**Channel A DRAM even Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated 001: Reserved 010: 4KB 011: 8KB 100: 16KB Others: Reserved

5.1.6 C0DRA2 – Channel A DRAM Rank 2, 3 Attribute

MMIO Range: MCHBAR
Address Offset: 109h
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.1.7 C0DCLKDIS – Channel A DRAM Clock Disable

MMIO Range: MCHBAR
Address Offset: 10Ch
Size: 8 bits

This register can be used to disable the System Memory Clock signals to each DIMM slot, which can significantly reduce EMI and Power concerns for clocks that go to unpopulated DIMMs. Clocks should be enabled based on whether a slot is populated, and what kind of DIMM is present.

Bit	Access & Default	Description
7:6		Reserved
5	R/W 0b	**DIMM clock gate enable pair 5:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
4	R/W 0b	**DIMM clock gate enable pair 4:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
3	R/W 0b	**DIMM clock gate enable pair 3:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
2	R/W 0b	**DIMM clock gate enable pair 2:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
1	R/W 0b	**DIMM clock gate enable pair 1:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
0	R/W 0b	**DIMM clock gate enable pair 0:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.

Note: Since there are multiple clock signals assigned to each Rank of a DIMM, it is important to clarify exactly which Rank width field affects which clock signal:

Channel	Rank	Clocks Affected
0	0 or 1	SA_CK_2:0/ SA_CKB_2:0
0	2 or 3	SA_CK_5:3/ SA_CKB_5:3
1	0 or 1	SB_CK_2:0/ SB_CKB_2:0
1	2 or 3	SB_CK_5:3/ SB_CKB_5:3

5.1.8 C0BNKARC – Channel A DRAM Bank Architecture

PCI Device: MCHBAR
Function: 0
Address Offset: 10Eh
Size: 16 bits

This register is used to program the bank architecture for each Rank

Bit	Access & Default	Description
15:8		Reserved
7:6	R/W 00b	**Rank 3 Bank Architecture:** 00: 4 Bank. 01: 8 Bank. 1X: Reserved
5:4	R/W 00b	**Rank 2 Bank Architecture:** 00: 4 Bank. 01: 8 Bank. 1X: Reserved
3:2	R/W 00b	**Rank 1 Bank Architecture:** 00: 4 Bank. 01: 8 Bank. 1X: Reserved
1:0	R/W 00b	**Rank 0 Bank Architecture:** 00: 4 Bank. 01: 8 Bank. 1X: Reserved

5.1.9 C0DRT1 – Channel A DRAM Timing Register

MMIO Range: MCHBAR
Address Offset: 114h
Size: 32 bits

Bit	Access & Default	Description
31:24		Reserved
23:20	R/W 9 h	**Activate to Precharge delay (tRAS):** This bit controls the number of DRAM clocks for tRAS. Minimum recommendations are beside their corresponding encodings. 0h – 3h Reserved 4h – Fh Four to Fifteen Clocks respectively.

Bit	Access & Default	Description
19	RO 0b	**Reserved for Activate to Precharge Delay (tRAS) MAX:** It is required that the Panic Refresh timer be set to a value less than the Tras max. Based on this setting a Panic Refresh occurs before Tras Max expiration and closes all the banks. This bit controls the maximum number of clocks that a DRAM bank can remain open. After this time period, the DRAM controller will guarantee to pre-charge the bank. This time period may or may not be set to overlap with time period that requires a refresh to happen. The DRAM controller includes a separate tRAS-MAX counter for every supported bank. With a maximum of four ranks, and four banks per rank, there are 16 counters per channel. This will not handle 8 bank devices correctly such as 1Gb technology in DDR2. 0 = 120 micro-seconds 1 = Reserved NOTE: this register will become Read Only with a value of 0 if the design does not implement these counters. TRAS MAX is not required because a panic refresh will close all banks in a rank before Tras max expires.
18:10		Reserved
9:8	R/W 01b	**CASB Latency (tCL):** This value is programmable on DDR2 DIMMs. The value programmed here must match the CAS Latency of every DDR2 DIMM in the system. **DDR CL Encoding:** **00: 3** **01: 2.5** **10: 2** **11: Reserved** **DDR2 CL Encoding:** **00: 5** **01: 4** **10: 3** **11: Reserved**
7		Reserved
6:4	R/W 010b	**DRAM RAS to CAS Delay (tRCD):** This bit controls the number of clocks inserted between a row activate command and a read or write command to that row. **EncodingtRCD** 000: 2 DRAM Clocks 010: 4 DRAM Clocks 011: 5 DRAM Clocks 100 - 111: Reserved
3		Reserved
2:0	R/W 010b	**DRAM RAS Precharge (tRP):** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank. **EncodingtRP** 000: 2 DRAM Clocks 001: 3 DRAM Clocks 010: 4 DRAM Clocks 011: 5 DRAM Clocks 100 - 111: Reserved

5.1.10 C0DRC0 – Channel A DRAM Controller Mode 0

MMIO Range: MCHBAR
Address Offset: 120h
Size: 32 bits

Bit	Access & Default	Description
31:30		Reserved
29	R/W 0b	**Initialization Complete (IC):** This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28:11		Reserved
10:8	R/W 000b	**Refresh Mode Select (RMS):** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000: Refresh disabled 001: Refresh enabled. Refresh interval 15.6 µsec 010: Refresh enabled. Refresh interval 7.8 µsec 011: Refresh enabled. Refresh interval 3.9 µsec 100: Refresh enabled. Refresh interval 1.95 µsec 111: Refresh enabled. Refresh interval 64 clocks (fast refresh mode) Other: Reserved
7	RO 0b	Reserved
6:4	R/W 000b	**Mode Select (SMS):** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. 000: Post Reset state – When the MCH exits reset (power-up or otherwise), the mode select field is cleared to “000”. During any reset sequence, while power is applied and reset is active, the MCH deasserts all CKE signals. After internal reset is deasserted, CKE signals remain deasserted until this field is written to a value different than “000”. On this event, all CKE signals are asserted. During suspend, MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. As part of resume sequence, MCH will be reset – which will clear this bit field to “000” and maintain CKE signals deasserted. After internal reset is deasserted, CKE signals remain deasserted until this field is written to a value different than “000”. On this event, all CKE signals are asserted. During entry to other low power states (C3, S1), MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. During exit to normal mode, MCH signal triggers DRAM controller to exit Self-Refresh and resume normal operation without S/W involvement. 001: NOP Command Enable – All CPU cycles to DRAM result in a NOP command on the DRAM interface. 010: All Banks Pre-charge Enable – All CPU cycles to DRAM result in an “all banks precharge” command on the DRAM interface. 011: Mode Register Set Enable – All CPU cycles to DRAM result in a “mode register” set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent. Host address lines [12:3] are mapped to MA[9:0], and HA[13] is mapped to MA[11]. 101: Reserved 110: CBR Refresh Enable – In this mode all CPU cycles to DRAM result in a CBR cycle on the DRAM interface 111: Normal operation

Bit	Access & Default	Description
3:2		Reserved
1:0	RO	**DRAM Type (DT):** Used to select between supported SDRAM types. 00: Reserved 01: Dual Data Rate (DDR) SDRAM 10: Second Revision Dual Data Rate (DDR2) SDRAM 11: Reserved

5.1.11 C1DRB0 – Channel B DRAM Rank Boundary Address 0

MMIO Range: MCHBAR
Address Offset: 180h
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.12 C1DRB1 – Channel B DRAM Rank Boundary Address 1

MMIO Range: MCHBAR
Address Offset: 181h
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.13 C1DRB2 – Channel B DRAM Rank Boundary Address 2

MMIO Range: MCHBAR
Address Offset: 182h
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.14 C1DRB3 – Channel B DRAM Rank Boundary Address 3

MMIO Range: MCHBAR
Address Offset: 183h
Size: 8 bits
The operation of this register is detailed in the description for register C0DRB0.

5.1.15 C1DRA0 – Channel B Dram Rank 0,1 Attribute

MMIO Range: MCHBAR
Address Offset: 188h
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.1.16 C1DRA2 – Channel B Dram Rank 2,3 Attribute

MMIO Range: MCHBAR
Address Offset: 189h
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.1.17 C1DCLKDIS – Channel B DRAM Clock Disable

MMIO Range: MCHBAR
Address Offset: 18Ch
Size: 8 bits

The operation of this register is detailed in the description for register C0DCLKDIS.

5.1.18 C1BNKARC – Channel B Bank Architecture

MMIO Range: MCHBAR
Address Offset: 18Eh
Size: 16 bits

The operation of this register is detailed in the description for register C0BNKARC.

5.1.19 C1DRT1 – Channel B DRAM Timing Register 1

MMIO Range: MCHBAR
Address Offset: 194h
Size: 32 bits

The operation of this register is detailed in the description for register C0DRT1.

5.1.20 C1DRC0 – Channel B DRAM Controller Mode 0

MMIO Range: MCHBAR
Address Offset: 1A0h
Size: 32 bits

The operation of this register is detailed in the description for register C0DRC0.

5.1.21 PMC2C3TT – C2 to C3 Transition Timer

PCI Device: MCHBAR
Address Offset: F00h
Size: 32 bits

Bit	Access & Default	Description
31:19		Reserved
18:7	R/W 000h	**C2 to C3 Transition Timer:** Number of core clocks to wait between last snoop and a transition from C2 to C3. Number of clocks waited in increments of 128 host common clocks. The value in this register is the maximum that the hclk phase counter reaches before returning to 0. In legacy power management mode this represents the amount of time to leave BM_BUSY# signal asserted after receiving a snoop message from the Hunit.
6:0		Reserved

5.1.22 PMC3C4TT – C3 to C4 Transition Timer

PCI Device: MCHBAR
Address Offset: F04h
Size: 32 bits

Bit	Access & Default	Description
31:19		Reserved
18:7	R/W 000h	**C3 to C4 Transition Timer:** Number of core clocks to wait between last snoop and a transition from C3 to C4. Number of clocks waited in increments of 128 host common clocks. The value in this register is the maximum that the hclk phase counter reaches before returning to 0. This field is not used when operating with the optional legacy power management mode
6:0		Reserved

5.1.23 PMSLFRFC – DRAM Self Refresh Control

PCI Device: MCHBAR
Address Offset: F08h
Size: 16 bits

Bit	Access & Default	Description
15	R/W 0b	**Global Self Refresh Enable:** 0 = Self Refresh Entry Disabled. 1 = Self Refresh Entry Global Enable. Bits 7:0 are applicable only if Global Enable is set to a 1.
14	R/W 0b	**Ignore Internal Graphics display restrictions:** 0 = Do not enter self refresh if internal graphics display subsystem requires the memory to be on all the time. 1 = Ignore Internal graphics display hardware and enter self refresh when all other conditions are satisfied.
13	R/W 0b	**Ignore Internal Graphics Render restrictions:** 0 = Do not enter self-refresh till internal graphics render engines are idle. 1 = Ignore Internal graphics render engine and enter self-refresh when all other conditions are satisfied.
12:7		Reserved
6:4	R/W 000b	**Self Refresh Processor State Dependency:** Defines when self-refresh is allowed based on the processor's ACPI C state. This field only defines the processor state conditions that must be met to use dynamic self-refresh. 000: Not allowed in C0, C1, C2, C3, or C4. 001: Reserved 010: Reserved 011: Reserved 100: Allowed in C4 only 101: Reserved 110: Allowed in C3 and C4 only 111: Allowed in C2, C3, and C4
3:2		Reserved
1:0	R/W 00b	**Self refresh Link State Dependency:** Defines when self-refresh is allowed based on the PCI Express* link states for both the graphics attached the ICH6 interface. This field only defines the link state conditions that must be met to use dynamic self-refresh. 00: Not allowed in L0, L0s or L1. 01: Reserved 10: Allowed in L1 only 11: Allowed in either L0s or L1

5.1.24 PMCFG – Power Management Configuration

PCI Device: MCHBAR
Address Offset: F10h
Size: 32 bits

Bit	Access & Default	Description
31:5		Reserved
4	R/W 0b	**Enhanced Power Management Features Enable:** 0 = Legacy power management mode 1 = Use enhanced power management When this bit is clear (default), the MCH must ignore the snoop timers for the purpose of deferring C state entry. In this mode the BM_BUSY# bit will be driven to the ICH6 beginning when any snoop activity is detected and held asserted for the duration described by the C2 to C3 snoop timer. When this bit is set, the MCH can use the snoop timers for determining the proper time for allowing a power management mode transition that was requested by ACPI software. When this bit is set the BM_BUSY# bit is never asserted. The Enhanced Power Management Mode and the Enhanced Power Management Snoop-detect Behavior fields may restrict the allowed behavior in this mode.
3	R/W 0b	**Enhanced Power Management Snoop-detect Behavior:** 0 = Snoop detection causes a request for C2 1 = Snoop detection causes a request for C0
2		**Reserved**
1:0	R/W 0b	**Enhanced Power Management Mode:** This field is ignored if the Enhanced Power Management Features Enable bit is cleared 00: All enhanced power management functions allowed 01: Disable the C2 to C3 snoop timer based transition. Never go past C2. 10: Disable the C3 to C4 snoop timer based transition. Never go past C3. 11: Reserved

5.1.25 PMSTS – Power Management Status

PCI Device: MCHBAR
Address Offset: F14h
Size: 32 bits

This register is Reset by PWROK only.

Bit	Access & Default	Description
31:2		Reserved
1	R/WC/S 0b	**Channel B in self-refresh:** Set by power management hardware after Channel B is placed in self refresh as a result of a Power State or a Reset Warn sequence. Cleared by Power management hardware before starting Channel B self refresh exit sequence initiated by a power management exit. Cleared by the BIOS in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 = Channel B not guaranteed to be in self-refresh. 1 = Channel B in Self-Refresh.
0	R/WC/S 0b	**Channel A in Self-refresh:** Set by power management hardware after Channel A is placed in self refresh as a result of a Power State or a Reset Warn sequence. Cleared by Power management hardware before starting Channel A self refresh exit sequence initiated by a power management exit. Cleared by the BIOS in a warm reset (Reset# asserted while PRWOK is asserted) exit sequence. 0 = Channel A not guaranteed to be in self-refresh. 1 = Channel A in Self-Refresh.

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6 EPBAR Registers – Egress Port Register Summary

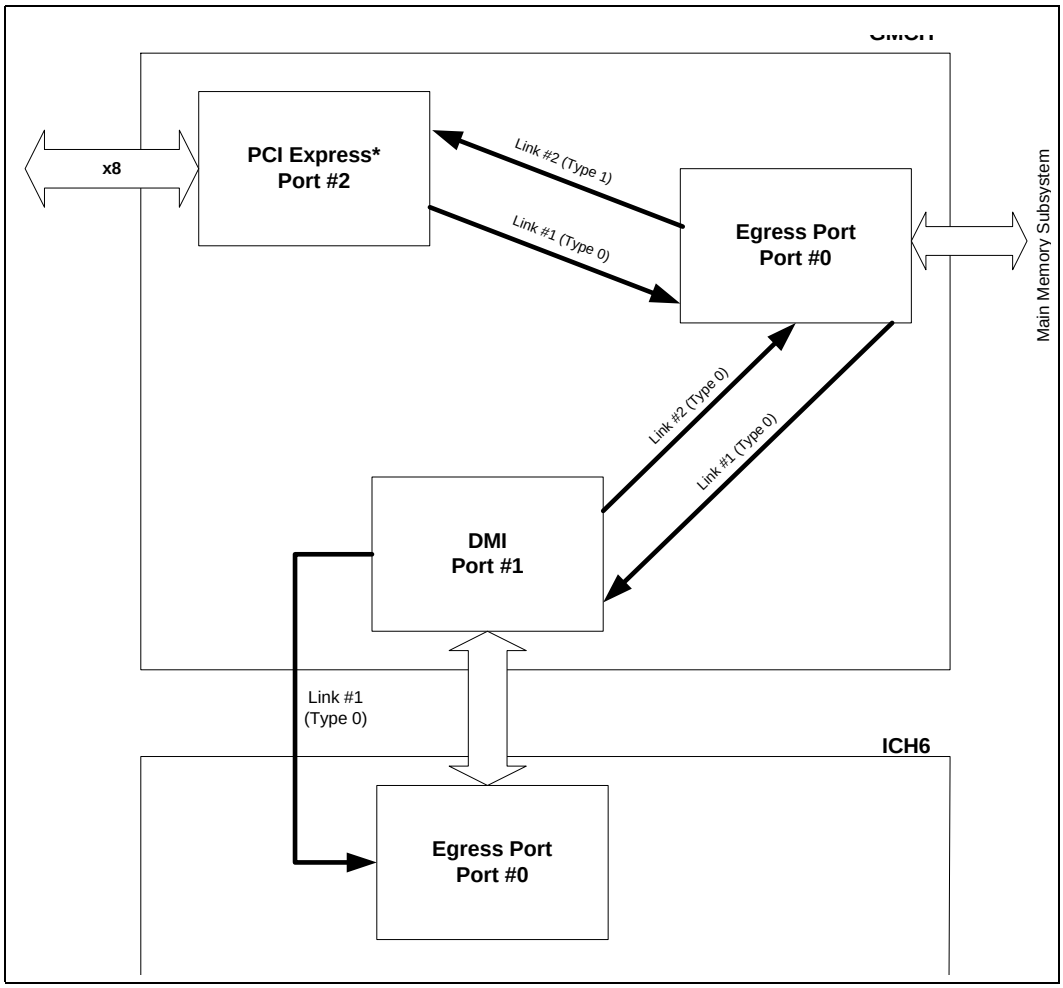
These registers are offset from the EPBAR base address.

Table 6-1. Egress Port Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
044h-047h	EPESD	EP Element Self Description	0000h	R/WO, RO
050h-053h	EPLE1D	EP Link Entry 1 Description	0100h	R/WO, RO
058h-05Fh	EPLE1A	EP Link Entry 1 Address	0000000000000000h	R/WO, RO
060h-063h	EPLE2D	EP Link Entry 2 Description	02000002h	R/WO, RO
068h-06Fh	EPLE2A	EP Link Entry 2 Address	0000000000008000h	RO

6.1 EP RCRB Configuration Register Details

Figure 6-1. Link Declaration Topology



6.1.1 EPESD – EP Element Self Description

MMIO Range: EPBAR
Address Offset: 044h
Size: 32 bits

Provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 00h	**Port Number:** This field specifies the port number associated with this element with respect to the component that contains this element. Value of 00h indicates to configuration software that this is the default egress port.
23:16	R/WO 00h	**Component ID:** Identifies the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 02h	**Number of Link Entries:** Indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PCI Express* and DMI).
7:4		Reserved
3:0	RO 1h	**Element Type:** Indicates the type of the Root Complex Element. Value of 1h represents a port to system memory.

6.1.2 EPLE1D – EP Link Entry 1 Description

MMIO Range: EPBAR
Address Offset: 050h
Size: 32 bits

First part of a Link Entry, which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 01h	**Target Port Number:** Specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 0b	**Link Type:** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid:** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

6.1.3 EPLE1A – EP Link Entry 1 Address

MMIO Range: EPBAR
Address Offset: 058h
Size: 64 bits

Second part of a Link Entry, which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32		Reserved
31:12	R/WO 00000h	**Link Address:** Memory mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0		Reserved

6.1.4 EPLE2D – EP Link Entry 2 Description

MMIO Range: EPBAR
Address Offset: 060h
Size: 32 bits

First part of a Link Entry, which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 02h	**Target Port Number:** Specifies the port number associated with the element targeted by this link entry. The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 1b	**Link Type:** Indicates that the link points to configuration space of the integrated device which controls the x8 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	R/WO 0b	**Link Valid** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

6.1.5 EPLE2A – EP Link Entry 2 Address

MMIO Range: EPBAR
Address Offset: 068h
Size: 64 bits

Second part of a Link Entry, which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:28		Reserved
27:20	RO 00h	Bus Number
19:15	RO 00001b	**Device Number:** Target for this link is PCI Express x8 port (Device 1).
14:12	RO 000b	Function Number
11:0		Reserved

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7 DMIBAR Registers – Direct Media Interface (DMI) RCRB

This Root Complex Register Block (RCRB) controls the MCH-Intel ICH6 serial interconnect. The base address of this space is programmed in DMIBAR in Device #0 config space. These registers are offset from the DMIBAR base address.

Warning: IMPORTANT: All RCRB register spaces need to remain organized as they are here.

Table 7-1. DMI Register Address Map Summary

Address Offset	Register Symbol	Register Name	PCI Dev #
000–003	DMIVCECH	DMI Virtual Channel Enhanced Capability Header	DMIBAR
004–007	DMIPVCCAP1	DMI Port VC Capability Register 1	DMIBAR
008–00B	DMIPVCCAP2	DMI Port VC Capability Register 2	DMIBAR
00C–00D	DMIPVCCTL	DMI Port VC Control	DMIBAR
00E–00F	—	Reserved	DMIBAR
010–013	DMIVC0RCAP	DMI VC0 Resource Capability	DMIBAR
014–017	DMIVC0RCTL	DMI VC0 Resource Control	DMIBAR
018–019	—	Reserved	DMIBAR
01A–01B	DMIVC0RSTS	DMI VC0 Resource Status	DMIBAR
01C–01F	DMIVC1RCAP	DMI VC1 Resource Capability	DMIBAR
020–023	DMIVC1RCTL	DMI VC1 Resource Control	DMIBAR
024–025	—	Reserved	DMIBAR
026–027	DMIVC1RSTS	DMI VC1 Resource Status	DMIBAR
028–083	—	Reserved	DMIBAR
084–087	DMILCAP	DMI Link Capabilities	DMIBAR
088–089	DMILCTL	DMI Link Control	DMIBAR
08A–08B	DMILSTS	DMI Link Status	DMIBAR
08C–FFF	—	Reserved	DMIBAR

7.1 DMI RCRB Configuration Register Details

7.1.1 DMIVCECH – DMI Virtual Channel Enhanced Capability Header

MMIO Range: DMIBAR
Address Offset: 000h
Size: 32 bits

Indicates DMI Virtual Channel capabilities.

Bit	Access & Default	Description
31:20	RO 040h	**Pointer to Next Capability:** Indicates the next item in the list.
19:16	RO 1h	**Capability Version:** Indicates support as a version 1 capability structure.
15:0	RO 0002 h	**Capability ID:** Indicates this is the Virtual Channel capability item.

7.1.2 DMIPVCCAP1 – DMI Port VC Capability Register 1

MMIO Range: DMIBAR
Address Offset: 004h
Size: 32 bits

Describes the configuration of Virtual Channels associated with this port.

Bit	Access & Default	Description
31:12		Reserved
11:10	RO 00b	**Port Arbitration Table Entry Size (PATS):** Indicates the size of the port arbitration table is 4-bits (to allow up to 8 ports):
9:8	RO 00b	**Reference Clock (RC):** Fixed at 100 ns.
7		Reserved
6:4	RO 000b	**Low Priority Extended VC Count (LPEVC):** Indicates that there are no additional VCs of low priority with extended capabilities.
3		Reserved
2:0	R/WO 001b	**Extended VC Count:** Indicates that there is one additional VC (VC1) that exists with extended capabilities.

7.1.3 DMIPVCCAP2 – DMI Port VC Capability Register 2

MMIO Range: DMIBAR
Address Offset: 008h
Size: 32 bits

Describes the configuration of Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset (ATO):** Indicates that no table is present for VC arbitration since it is fixed.
23:8		Reserved
7:0	RO 01h	**VC Arbitration Capability.** Indicates that the VC arbitration is fixed in the root complex. VC1 is highest priority and VC0 is lowest priority.

7.1.4 DMIPVCCTL – DMI Port VC Control

MMIO Range: DMIBAR
Address Offset: 00Ch
Size: 16 bits

Bit	Access & Default	Description
15:4		Reserved
3:1	R/W 000b	**VC Arbitration Select:** Indicates which VC should be programmed in the VC arbitration table. The root complex takes no action on the setting of this field since there is no arbitration table.
0	RO 0b	**Load VC Arbitration Table (LAT):** Indicates that the table programmed should be loaded into the VC arbitration table. This bit is defined as read/write with always returning 0 on reads.

7.1.5 DMIVC0RCAP – DMI VC0 Resource Capability

MMIO Range: DMIBAR
Address Offset: 010h
Size: 32 bits

Bit	Access & Default	Description
31:24	RO 00h	**Port Arbitration Table Offset (AT):** This VC implements no port arbitration table since the arbitration is fixed.
23		Reserved
22:16	RO 00h	**Maximum Time Slots (MTS):** This VC implements fixed arbitration, and therefore this field is not used.
15	RO 0b	**Reject Snoop Transactions (RTS):** This VC must be able to take snoopable transactions.
14	RO 0b	**Advanced Packet Switching (APS):** This VC is capable of all transactions, not just advanced packet switching transactions.

Bit	Access & Default	Description
13:8		Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** Indicates that this VC uses fixed port arbitration.

7.1.6 DMIVC0RCTL0 – DMI VC0 Resource Control

MMIO Range: DMIBAR
Address Offset: 014h
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:27		Reserved
26:24	RO 000b	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel.
23:20		Reserved
19:17	R/W 0h	**Port Arbitration Select (PAS):** Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16	RO 0b	**Load Port Arbitration Table (LAT):** The root complex does not implement an arbitration table for this virtual channel.
15:8		Reserved
7:1	R/W 7F h	**Transaction Class / Virtual Channel Map (TVM):** RW. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0		Reserved

7.1.7 DMIVC0RSTS – DMI VC0 Resource Status

MMIO Range: DMIBAR
Address Offset: 01Ah
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1b	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
0	RO 0b	**Port Arbitration Tables Status (ATS):** There is no port arbitration table for this VC, so this bit is reserved at 0.

7.1.8 DMIVC1RCAP – DMI VC1 Resource Capability

MMIO Range: DMIBAR
Address Offset: 01Ch
Size: 32 bits

Bit	Access & Default	Description
31:24	RO 00h	**Port Arbitration Table Offset (AT):** Indicates the location of the port arbitration table in the root complex. A value of 3h indicates the table is at offset 30h.
23		Reserved
22:16	RO 00h	**Maximum Time Slots (MTS):** This value is updated by platform BIOS based upon the determination of the number of time slots available in the platform.
15	RO 1b	**Reject Snoop Transactions (RTS):** All snoopable transactions on VC1 are rejected. This VC is for isochronous transfers only.
14	RO 0b	**Advanced Packet Switching (APS):** This VC is capable of all transactions, not just advanced packet switching transactions.
13:8		Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** Indicates the port arbitration capability is time-based WRR of 128 phases.

7.1.9 DMIVC1RCTL1 – DMI VC1 Resource Control

MMIO Range: DMIBAR
Address Offset: 020h
Size: 32 bits

Controls the resources associated with Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0b	**Virtual Channel Enable (EN):** R/W. Enables the VC when set. Disables the VC when cleared.
30:27	RO 0h	Reserved
26:24	R/W 001b	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel.
23:20		Reserved
19:17	R/W 0h	**Port Arbitration Select (PAS):** Indicates which port table is being programmed. The only permissible value of this field is 4h for the time-based WRR entries.
16	RO 0b	**Load Port Arbitration Table (LAT):** When set, the port arbitration table loaded based upon the PAS field in this register. This bit always returns 0 when read.
15:8		Reserved
7:1	R/W 00h	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0		Reserved

7.1.10 DMIVC1RSTS – DMI VC1 Resource Status

MMIO Range: DMIBAR
Address Offset: 026h
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 0b	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
0	RO 0b	**Port Arbitration Tables Status (ATS):** Indicates the coherency status of the port arbitration table. This bit is set when LAT (offset 000Ch:bit 0) is written with value '1' and PAS (offset 0014h:bits19:17) has value of 4h. This bit is cleared after the table has been updated.

7.1.11 DMILCAP – DMI Link Capabilities

MMIO Range: DMIBAR
Address Offset: 084h
Size: 32 bits

Indicates DMI specific capabilities.

Bit	Access & Default	Description
31:18		Reserved
17:15	R/WO 010b	**L1 Exit Latency (EL1):** L1 not supported on DMI.
14:12	R/WO 010b	**L0s Exit Latency (EL0):** This field indicates that exit latency is 128 ns to less than 256 ns.
11:10	RO 11b	**Active State Link PM Support (APMS):** Indicates that L0s is supported on DMI.
9:4	RO 4 h	**Maximum Link Width (MLW):** Indicates the maximum link width is 4 ports.
3:0	RO 1h	**Maximum Link Speed (MLS):** Indicates the link speed is 2.5 Gb/s.

7.1.12 DMILCTL – DMI Link Control

MMIO Range: DMIBAR
Address Offset: 088h
Size: 16 bits

Allows control of DMI.

Bit	Access & Default	Description
15:8		Reserved
7	R/W 0h	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets when exiting L0s prior to entering L0 and extra TS1 sequences at exit from L1 prior to entering L0.
6:2		Reserved
1:0	R/W 00b	**Active State Link PM Control (APMC):** Indicates whether DMI should enter L0s. 00 = Disabled 01 = L0s entry enabled 10 = Reserved 11 = Reserved

7.1.13 DMILSTS – DMI Link Status

MMIO Range: DMIBAR
Address Offset: 08Ah
Size: 16 bits

Indicates DMI status.

Bit	Access & Default	Description
15:10		Reserved
9:4	RO 00h	**Negotiated Link Width (NLW):** Negotiated link width is x4 (000100b).
3:0	RO 1h	Link Speed (LS). Link is 2.5 Gb/s

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8 Device 1 Host – PCI Express Bridge Registers (D1:F0)

Device 1 contains the controls associated with the PCI Express x8 root port that is the intended to attach as the point for Intel® 6702PXH 64-bit PCI Hub. In addition, it also functions as the virtual PCI-to-PCI Bridge.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express Specification* defines two types of reserved bits: Reserved and Preserved.

1. Reserved for future RW implementations; software must preserve value read for writes to bits.
2. Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type, which have historically been the typical definition for Reserved.

It is important to note that most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first Disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

Table 8-1. Device 1 Register Summary (Sheet 1 of 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
00-01h	VID1	Vendor Identification	8086h	RO
02-03h	DID1	Device Identification	2589h	RO
04-05h	PCICMD1	PCI Command	0000h	RO, R/W
06-07h	PCISTS1	PCI Status	0000h	RO, R/W
08h	RID1	Revision Identification	00h	RO
09-0Bh	CC1	Class Code	060400h	RO
0Ch	CL1	Cache Line Size	00h	R/W
0Dh	—	**Reserved**	—	—
0Eh	HDR1	Header Type	01h	RO
0F-17h	—	**Reserved**	—	—
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	RO
1Ah	SUBUSN1	Subordinate Bus Number	00h	R/W
1Bh	—	**Reserved**	—	—
1Ch	IOBASE1	I/O Base Address	F0h	RO
1Dh	IOLIMIT1	I/O Limit Address	00h	R/W
1Eh-1Fh	SSTS1	Secondary Status	00h	RO, R/W/C

Table 8-1. Device 1 Register Summary (Sheet 2 of 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
20-21h	MBASE1	Memory Base Address	FFF0h	R/W
22-23h	MLIMIT1	Memory Limit Address	0000h	R/W
24-25h	PMBASE1	Prefetchable Memory Base Address	FFF0h	RO, R/W
26-27h	PMLIMIT1	Prefetchable Memory Limit Address	0000h	RO, R/W
28-33h	—	**Reserved**	—	—
34h	CAPPTR1	Capabilities Pointer	88h	RO
35-3Bh	—	**Reserved**	—	—
3Ch	INTRLINE1	Interrupt Line	00h	R/W
3Dh	INTRPIN1	Interrupt Pin	00h	RO
3E-3Fh	BCTRL1	Bridge Control	0000h	RO, R/W
40-7Fh	—	**Reserved**	—	—
80-83h	PM_CAP1	Power Management Capabilities	1902 9/A 001h	RO
84-87h	PM_CS1	Power Management Control/Status	00000000h	RO, R/W/S
88-8Bh	SS_CAPID	Subsystem ID and Vendor ID Capabilities	0000800Dh	RO
8C-8Fh	SS	Subsystem ID and Subsystem Vendor ID	00008086h	RO
90-91h	MSI_CAPID	Message Signaled Interrupts Capability ID	A005h	RO
92-93h	MC	Message Control	0000h	RO, R/W
94-97h	MA	Message Address	00000000h	RO, R/W
98-99h	MD	Message Data	0000h	R/W
9A-9Fh	—	**Reserved**	—	—
A0-A1h	PEG_CAPL	PCI Express* Capability List	0010h	RO
A2-A3h	PEG_CAP	PCI Express Capabilities	0141h	RO
A4-A7h	DCAP	Device Capabilities	00000000h	RO
A8-A9h	DCTL	Device Control	0000h	R/W
AA-ABh	DSTS	Device Status	0000h	RO
AC-AFh	LCAP	Link Capabilities	02012E01h	R/WO
B0-B1h	LCTL	Link Control	0000h	RO, R/W
B2-B3h	LSTS	Link Status	1001h	RO
B4-B7h	SLOTCAP	Slot Capabilities	00000000h	R/WO
B8-B9h	SLOTCTL	Slot Control	0000h	RO, R/W
BA-BBh	SLOTSTS	Slot Status	0000h	RO, R/W/C
B4-BBh	—	**Reserved**	—	—
BC-BDh	RCTL	Root Control	0000h	R/W
BE-BFh	—	**Reserved**	—	—
C0-C3h	RSTS	Root Status	00000000h	RO, R/W/C
C4-EB	—	**Reserved**	—	—
EC-EFh	PEGLC	PCI Express Legacy Control	00000000h	RO, R/W

Table 8-1. Device 1 Register Summary (Sheet 3 of 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
F0-FFh	—	**Reserved**	—	—
100-103h	VCECH	Virtual Channel Enhanced Capability Header	14010002h	RO
104-107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO, R/WO
108-10Bh	PVCCAP2	Port VC Capability Register 2	00000001h	RO
10C-10Dh	PVCCTL	Port VC Control	0000h	R/W
10E-10Fh	—	**Reserved**	—	—
110-113h	VC0RCAP	VC0 Resource Capability	00000000h	RO
114-117h	VC0RCTL	VC0 Resource Control	8000007Fh	RO, R/W
118-119h	—	**Reserved**	—	—
11A-11Bh	VC0RSTS	VC0 Resource Status	0000h	RO
11C-11Fh	VC1RCAP	VC1 Resource Capability	00008000h	RO
120-123h	VC1RCTL	VC1 Resource Control	01000000h	RO, R/W
124-125h	—	**Reserved**	—	—
126-127h	VC1RSTS	VC1 Resource Status	0000h	RO
128-13Fh	—	**Reserved**	—	—
140-143h	RCLDECH	Root Complex Link Declaration Enhanced Capability Header	000/1C0 1005h	RO
144-147h	ESD	Element Self Description	02000100h	RO, R/WO
148-14Fh	—	**Reserved**	—	—
150-153h	LE1D	Link Entry 1 Description	00000000h	RO, R/WO
154-157h	—	**Reserved**	—	—
158-15Fh	LE1A	Link Entry 1 Address	0000000000 000000h	R/WO
160-217h	—	**Reserved**	—	—
218-21F	PEGSSTS	PCI Express Sequence Status	0000000000 000000h	RO
220-FFFh	—	**Reserved**	—	—

8.1 Device 1 Configuration Register Details

8.1.1 VID1 – Vendor Identification (D1:F0)

PCI Device: 1
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification (VID1):** PCI standard identification for Intel.

8.1.2 DID1 – Device Identification (D1:F0)

PCI Device: 1
Address Offset: 02h
Default Value: 2589h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2589h	**Device Identification Number (DID1):** Identifier assigned to the MCH Device 1 (virtual PCI-to-PCI bridge, PCI Express* port).

8.1.3 PCICMD1 – PCI Command (D1:F0)

PCI Device: 1
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:11		Reserved
10	R/W 0b	**INTA Assertion Disable:** Any INTA emulation interrupts already asserted must be deasserted when this bit is set. 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD asserts and deassert messages.

Bit	Access & Default	Description
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** Not Applicable or Implemented. Hardwired to 0.
8	R/W 0b	**SERR Message Enable (SERRE1):** This bit is an enable bit for Device 1 SERR messaging. The MCH communicates the SERRB condition by sending an SERR message to the ICH6. This bit, when set, enables reporting of non-fatal and fatal errors to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI Express* specific bits in the Device Control Register 0 = The SERR message is generated by the MCH for Device 1 only under conditions enabled individually through the Device Control Register. 1 = The MCH is enabled to generate SERR messages which will be sent to the ICH6 for specific Device 1 error conditions that are individually enabled in the BCTRL1 register and for all non-fatal and fatal errors generated on the primary side of the virtual PCI to PCI Express bridge (not those received by the secondary side). The error status is reported in the PCISTS1 register.
7	RO 0b	Reserved
6	RO 0b	**Parity Error Enable (PERRE):** Controls whether or not the Master Data Parity Error bit in the PCI Status register can be set. 0 = Master Data Parity Error bit in PCI Status register can NOT be set. 1 = Master Data Parity Error bit in PCI Status register CAN be set.
5	RO 0b	**VGA Palette Snoop:** Not Applicable or Implemented. Hardwired to 0.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Not Applicable or Implemented. Hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** Not Applicable or Implemented. Hardwired to 0.
2	R/W 0b	**Bus Master Enable (BME):** This bit does not affect forwarding of Completions from the primary interface to the secondary interface. 0 = This device is prevented from making memory or IO requests to its primary bus. Note that according to the *PCI Specification*, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/reads, peer writes/reads, and MSIs will all be treated as illegal cycles. Writes are forwarded to memory address 0 with byte enables deasserted. Reads will be forwarded to memory address 0 and will return Unsupported Request status (or Master abort) in its completion packet. 1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available.
1	R/W 0b	**Memory Access Enable (MAE)** 0 = All of Device 1's memory space is disabled. 1 = Enable the Memory and Prefetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	R/W 0b	**IO Access Enable (IOAE)** 0 = All of Device 1's I/O space is disabled. This bit does not affect forwarding of Completions from the primary interface to the secondary interface.nable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

8.1.4 PCISTS1 – PCI Status (D1:F0)

PCI Device: 1
Address Offset: 06h
Default Value: 0000h
Access: RO, R/W/C
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express Bridge embedded within the MCH.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Not Applicable or Implemented. Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device (we don't perform error forwarding).
14	R/WC 0b	**Signaled System Error (SSE):** This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO 0b	**Received Master Abort Status (RMAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO 0b	**Received Target Abort Status (RTAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO 0b	**Signaled Target Abort Status (STAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO 00b	**DEVSELB Timing (DEVT):** This device is not the subtractive decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO 0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PCI Express* virtual P2P bridge is integrated with the MCH functionality there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as a R/WC, but for our implementation an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO 0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6		Reserved
5	RO 0b	**66/60 MHz capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4	RO 1b	**Capabilities List:** Indicates that a capabilities list is present. Hardwired to 1.
3	RO 0b	**INTA Status:** Indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and deassert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit. Note that INTA emulation interrupts received across the link are not reflected in this bit.
2:0		Reserved

8.1.5 RID1 – Revision Identification (D1:F0)

PCI Device: 1
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number of the MCH Device 1. These bits are read only and writes to this register have no effect.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID1):** Indicates the number of times that this device in this component has been “stepped” through the manufacturing process. It is always the same as the RID values in all other devices in this component. For the A-0 Stepping, this value is 00h.

8.1.6 CC1 – Class Code (D1:F0)

PCI Device: 1
Address Offset: 09h
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** Indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.
15:8	RO 04h	**Sub-Class Code (SUBCC):** Indicates the sub-class code for this device. The code is 04h indicating a PCI-to-PCI Bridge.
7:0	RO 00h	**Programming Interface (PI):** Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

8.1.7 CL1 – Cache Line Size (D1:F0)

PCI Device: 1
Address Offset: 0Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00h	**Cache Line Size (Scratch pad):** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express* device functionality.

8.1.8 HDR1 – Header Type (D1:F0)

PCI Device: 1
Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 01h	**Header Type Register (HDR):** Returns 01 to indicate that this is a single function device with bridge header layout.

8.1.9 PBUSN1 – Primary Bus Number (D1:F0)

PCI Device: 1
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this “virtual” Host-PCI Express bridge is connected to PCI bus 0.

Bit	Access & Default	Description
7:0	RO 00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since Device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

8.1.10 SBUSN1 – Secondary Bus Number (D1:F0)

PCI Device: 1
Address Offset: 19h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the “virtual” bridge i.e. to PCI Express. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express.

Bit	Access & Default	Description
7:0	R/W 00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express*.

8.1.11 SUBUSN1 – Subordinate Bus Number (D1:F0)

PCI Device: 1
Address Offset: 1Ah
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express.

Bit	Access & Default	Description
7:0	R/W 00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the Device 1 bridge. When only a single PCI device resides on the PCI Express* segment, this register will contain the same value as the SBUSN1 register.

8.1.12 IOBASE1 – I/O Base Address (D1:F0)

PCI Device: 1
Address Offset: 1Ch
Default Value: F0h
Access: RO
Size: 8 bits

This register controls the processor to PCI Express I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A [11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4KB boundary.

Bit	Access & Default	Description
7:4	R/W Fh	**I/O Address Base (IOBASE):** Corresponds to A [15:12] of the I/O addresses passed by bridge 1 to PCI Express. BIOS must not set this register to 00h otherwise 0CF8h/0CFCh accesses will be forwarded to the PCI Express* hierarchy associated with this device.
3:0		Reserved

8.1.13 IOLIMIT1 – I/O Limit Address (D1:F0)

PCI Device: 1
Address Offset: 1Dh
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the processor to PCI Express I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only upper 4 bits are programmable. For the purposes of address decode address bits A [11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4KB aligned address block.

Bit	Access & Default	Description
7:4	R/W 0h	**I/O Address Limit (IOLIMIT):** Corresponds to A[15:12] of the I/O address limit of Device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express* hierarchy associated with this device.
3:0		Reserved

8.1.14 SSTS1 – Secondary Status (D1:F0)

PCI Device: 1
Address Offset: 1Eh
Default Value: 00h
Access: RO, R/W/C
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e. PCI Express side) of the “virtual” PCI-PCI Bridge embedded within MCH.

Bit	Access & Default	Description
15	R/WC 0b	Reserved
14	R/WC 0b	**Received System Error (RSE):** This bit is set when the secondary side sends an ERR_FATAL or ERR_NONFATAL message due to an error detected by the secondary side, and the SERR Enable bit in the Bridge Control register is ‘1’.
13	R/WC 0b	**Received Master Abort (RMA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.
12	R/WC 0b	**Received Target Abort (RTA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.
11	RO 0b	**Signaled Target Abort (STA):** Not Applicable or Implemented. Hardwired to 0. The MCH does not generate Target Aborts (the MCH will never complete a request using the Completer Abort Completion status).
10:9	RO 00b	**DEVSELB Timing (DEVT):** Not Applicable or Implemented. Hardwired to 0.

Bit	Access & Default	Description
8	RO 0b	Reserved
7	RO 0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6		Reserved
5	RO 0b	**66/60 MHz capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4:0		Reserved

8.1.15 MBASE1 – Memory Base Address (D1:F0)

PCI Device: 1
Address Offset: 20h
Default Value: FFF0h
Access: R/W
Size: 16 bits

This register controls the processor to PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A [31:20] of the 32-bit address. The bottom 4-bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Memory Address Base (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express*.
3:0		Reserved

8.1.16 MLIMIT1 – Memory Limit Address (D1:F0)

PCI Device: 1
Address Offset: 22h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register controls the processor to PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A [31:20] of the 32-bit address. The bottom 4-bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor-to-PCI Express memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges i.e. prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Access & Default	Description
15:4	R/W 000h	**Memory Address Limit (MLIMIT):** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.
3:0		Reserved

8.1.17 PMBASE1 – Prefetchable Memory Base Address (D1:F0)

PCI Device: 1
Address Offset: 24h
Default Value: FFF0h
Access: RO, R/W
Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12-bits of this register are read/write and correspond to address bits A [31:20] of the 40-bit address. The lower 8-bits of the Upper Base Address register are read/write and correspond to address bits A [39:32] of the 40-bit address. The configuration software must initialize this register. For the purpose of address decodes address bits A [19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Prefetchable Memory Base Address (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express*.
3:0	RO 0h	**64-bit Address Support:** Indicates the bridge supports only 32-bit addresses.

8.1.18 PMLIMIT1 – Prefetchable Memory Limit Address (D1:F0)

PCI Device: 1
Address Offset: 26h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12-bits of this register are read/write and correspond to address bits A [31:20] of the 40-bit address. The lower 8-bits of the Upper Limit Address register are read/write and correspond to address bits A [39:32] of the 40-bit address. The configuration software must initialize this register. For the purpose of address decodes address bits A [19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the processor perspective.

Bit	Access & Default	Description
15:4	R/W 000h	**Prefetchable Memory Address Limit (PMLIMIT):** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express*.
3:0	RO 0h	**64-bit Address Support:** Indicates the bridge supports only 32-bit addresses.

8.1.19 CAPPTR1 – Capabilities Pointer (D1:F0)

PCI Device: 1
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access & Default	Description
7:0	RO 88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

8.1.20 INTRLINE1 – Interrupt Line (D1:F0)

PCI Device: 1
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value; rather device drivers and operating systems to determine priority and vector information use it.

Bit	Access & Default	Description
7:0	R/W 00h	**Interrupt Connection:** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller this device's interrupt pin is connected to.

8.1.21 INTRPIN1 – Interrupt Pin (D1:F0)

PCI Device: 1
Address Offset: 3Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin:** As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h = INTA

8.1.22 BCTRL1 – Bridge Control (D1:F0)

PCI Device: 1
Address Offset: 3Eh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e. PCI Express) as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge embedded within MCH, e.g. VGA compatible address ranges mapping.

Bit	Access & Default	Description
15:12		Reserved
11	RO 0b	**Discard Timer SERR Enable:** Not Applicable or Implemented. Hardwired to 0.

Bit	Access & Default	Description
10	RO 0b	**Discard Timer Status:** Not Applicable or Implemented. Hardwired to 0.
9	RO 0b	**Secondary Discard Timer:** Not Applicable or Implemented. Hardwired to 0.
8	RO 0b	**Primary Discard Timer:** Not Applicable or Implemented. Hardwired to 0.
7	RO 0b	**Fast Back-to-Back Enable (FB2BEN):** Not Applicable or Implemented. Hardwired to 0.
6	R/W 0b	**Secondary Bus Reset (SRESET):** Setting this bit triggers a hot reset on the corresponding PCI Express* port.
5	RO 0b	**Master Abort Mode (MAMODE):** When acting as a master, unclaimed reads that experience a master abort returns all 1's and any writes that experience a master abort completes normally and the data is thrown away. Hardwired to 0.
4		**VGA 16-bit Decode:** Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to '1', enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.
3	R/W 0b	**VGA Enable (VGAEN):** Controls the routing of processor initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in Device 0, offset 97h[0].
2	R/W 0b	**ISA Enable (ISAEN):** Needed to exclude legacy resource decode to route ISA resources to legacy decode path. Modifies the response by the MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI Express. 1 = MCH will not forward to PCI Express any I/O transactions addressing the last 768 bytes in each 1KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI Express these cycles will be forwarded to DMI where they can be subtractively or positively claimed by the ISA bridge.
1	R/W 0b	**SERR Enable (SERREN)** 0 = No forwarding of error messages from secondary side to primary side that could result in an SERR. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	RO 0b	**Parity Error Response Enable (PEREN):** Controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the MCH receives across the link (upstream) a Read Data Completion Poisoned TLP 0 = Master Data Parity Error bit in Secondary status register can NOT be set. 1 = Master Data Parity Error bit in Secondary status register CAN be set.

8.1.23 PM_CAPID1 – Power Management Capabilities (D1:F0)

PCI Device: 1
Address Offset: 80h
Default Value: 1902 9/A 001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:27	RO 19h	**PME Support:** This field indicates the power states in which this device may indicate PME wake via PCI Express* messaging. D0, D3hot, and D3cold. This device is not required to do anything to support D3hot and D3cold; it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details.
26	RO 0b	**D2:** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO 0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO 000b	**Auxiliary Current:** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO 0b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO 0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19	RO 0b	**PME Clock:** Hardwired to 0 to indicate this device does NOT support PMEB generation.
18:16	RO 010b	**PCI PM CAP Version:** Hardwired to 02h to indicate there are 4 bytes of power management registers implemented and that this device complies with Rev. 1.1 of the *PCI Power Management Interface Specification*.
15:8	RO 90h / A0h	**Pointer to Next Capability:** This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h. If MSICH (CAPL[0] @ 7Fh) is 1, then the next item in the capabilities list is the PCI Express capability at A0h.
7:0	RO 01h	**Capability ID:** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

8.1.24 PM_CS1 – Power Management Control/Status (D1:F0)

PCI Device: 1
Address Offset: 84h
Default Value: 00000000h
Access: RO, R/W/S
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 0b	**PME Status:** Indicates that this device does not support PMEB generation from $D3^{cold}$.

Bit	Access & Default	Description
14:13	RO 00b	**Data Scale:** Indicates that this device does not support the power management data register.
12:9	RO 0h	**Data Select:** Indicates that this device does not support the power management data register.
8	R/W/S 0b	**PME Enable:** Indicates that this device does not generate PMEB assertion from any D-state. 0 = PMEB generation not possible from any D State 1 = PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2		Reserved
1:0	R/W 00b	**Power State:** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00: D0 01: D1 (Not supported in this device.) 10: D2 (Not supported in this device.) 11: D3 Support of $D3_{cold}$ does not require any special action. While in the $D3_{hot}$ state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully functional. There is no hardware functionality required to support these Power States.

8.1.25 SS_CAPID – Subsystem ID and Vendor ID Capabilities (D1:F0)

PCI Device: 1
Address Offset: 88h
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access & Default	Description
31:16		Reserved
15:8	RO 80h	**Pointer to Next Capability:** This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO 0Dh	**Capability ID:** Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

8.1.26 SS – Subsystem ID and Subsystem Vendor ID (D1:F0)

PCI Device: 1
Address Offset: 8Ch
Default Value: 00008086h
Access: RO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and hardware reset.

Bit	Access & Default	Description
31:16	R/WO 0000h	**Subsystem ID (SSID):** Identifies the particular subsystem and is assigned by the vendor.
15:0	R/WO 8086h	**Subsystem Vendor ID (SSVID):** Identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.

8.1.27 MSI_CAPID – Message Signaled Interrupts Capability ID (D1:F0)

PCI Device: 1
Address Offset: 90h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

The reporting of the existence of this capability can be disabled by setting MSICH (CAPL [0] @ 7Fh). In that case walking this linked list will skip this capability and instead go directly from the PCI PM capability to the PCI Express capability.

Bit	Access & Default	Description
15:8	RO A0h	**Pointer to Next Capability:** This contains a pointer to the next item in the capabilities list which is the PCI Express* capability.
7:0	RO 05h	**Capability ID:** Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

8.1.28 MC – Message Control (D1:F0)

PCI Device: 1
Address Offset: 92h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access & Default	Description
15:8		Reserved
7	RO 0b	**64-bit Address Capable:** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32b/4GB limit.
6:4	R/W 000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO 000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. Value: Number of Messages Requested 000: 1 All other's are reserved in this implementation: 001: Reserved 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
0	R/W 0b	**MSI Enable (MSIEN) Controls the ability of this device to generate MSIs.** 0 = MSI will not be generated. 1 = MSI will be generated when we receive PME or Hot-Plug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

8.1.29 MA – Message Address (D1:F0)

PCI Device: 1
Address Offset: 94h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:2	R/W 00000000h	**Message Address:** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO 00b	**Force DWord Align:** Hardwired to 0 so that addresses assigned by system software are always aligned on a Dword address boundary.

8.1.30 MD – Message Data (D1:F0)

PCI Device: 1
Address Offset: 98h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	**Message Data:** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16-bits are always set to 0. This register supplies the lower 16-bits.

8.1.31 PEG_CAPL – PCI Express Capability List (D1:F0)

PCI Device: 1
Address Offset: A0h
Default Value: 0010h
Access: RO
Size: 16 bits

Enumerates the PCI Express capability structure.

Bit	Access & Default	Description
15:8	RO 00h	**Pointer to Next Capability:** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express* specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space.
7:0	RO 10h	**Capability ID:** Identifies this linked list item (capability structure) as being for PCI Express registers.

8.1.32 PEG_CAP – PCI Express Capabilities (D1:F0)

PCI Device: 1
Address Offset: A2h
Default Value: 0141h
Access: RO
Size: 16 bits

Indicates PCI Express device capabilities.

Bit	Access & Default	Description
15:14		Reserved
13:9	RO 00h	**Interrupt Message Number:** Not Applicable or Implemented. Hardwired to 0.
8	R/WO 1b	**Slot Implemented** 0 = The PCI Express* Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot. BIOS must initialize this field appropriately if a slot connection is not implemented.
7:4	RO 4h	**Device/Port Type:** Hardwired to 0100 to indicate root port of PCI Express Root Complex.
3:0	RO 1h	**PCI Express Capability Version:** Hardwired to 1 as it is the first version.

8.1.33 DCAP – Device Capabilities (D1:F0)

PCI Device: 1
Address Offset: A4h
Default Value: 00000000h
Access: RO
Size: 32 bits

Indicates PCI Express link capabilities.

Bit	Access & Default	Description
31:6		Reserved
5	RO 0b	**Extended Tag Field Supported:** Hardwired to indicate support for 5-bit Tags as a Requestor.
4:3	RO 00b	**Phantom Functions Supported:** Not Applicable or Implemented. Hardwired to 0.
2:0	RO 000b	**Max Payload Size:** Hardwired to indicate 128B max supported payload for Transaction Layer Packets (TLP).

8.1.34 DCTL – Device Control (D1:F0)

PCI Device: 1
Address Offset: A8h
Default Value: 0000h
Access: R/W
Size: 16 bits

Provides control for PCI Express device specific capabilities.

Note: The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access & Default	Description
15:8		Reserved
7:5	R/W 000b	**Max Payload Size** 000: 128B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. **NOTE:** All other encodings are reserved.
4		Reserved
3	R/W 0b	**Unsupported Request Reporting Enable:** When set Unsupported Requests will be reported. **NOTE:** Reporting of error messages received by Root Port is controlled exclusively by Root Control register.
2	R/W 0b	**Fatal Error Reporting Enable:** When set fatal errors will be reported. For a Root Port, the reporting of fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	R/W 0b	**Non-Fatal Error Reporting Enable:** When set non-fatal errors will be reported. For a Root Port, the reporting of non-fatal errors is internal to the root. No external ERR_NONFATAL message is generated. Uncorrectable errors can result in degraded performance.
0	R/W 0b	**Correctable Error Reporting Enable:** When set correctable errors will be reported. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_CORR message is generated.

8.1.35 DSTS – Device Status (D1:F0)

PCI Device: 1
Address Offset: AAh
Default Value: 0000h
Access: RO
Size: 16 bits

Reflects status corresponding to controls in the Device Control register.

Note: The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access & Default	Description
15:6		Reserved
5	RO 0b	**Transactions Pending** 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Indicates that the device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4		Reserved
3	R/WC 0b	**Unsupported Request Detected:** When set this bit indicates that the Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option, as support for AER will not be reported.
2	R/WC 0b	**Fatal Error Detected:** When set this bit indicates that fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
1	R/WC 0b	**Non-Fatal Error Detected:** When set this bit indicates that non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
0	R/WC 0b	**Correctable Error Detected:** When set this bit indicates that correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. The MCH may report a false 8B/10B Receiver Error when exiting L0s. This is reported thru the Correctable Error Detected bit CESTS device 1, offset 1D0h, Bit [0]. This will reduce the value of Receiver Error detection when L0s is enabled. Disable L0s for accurate Receiver Error reporting.

8.1.36 LCAP – Link Capabilities (D1:F0)

PCI Device: 1
Address Offset: ACh
Default Value: 02012C01h
Access: R/WO
Size: 16 bits

Indicates PCI Express device specific capabilities.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number:** Indicates the PCI Express* port number for the given PCI Express link. Matches the value in Element Self Description [31:24].
23:18		Reserved
17:15	R/WO 010b	**L1 Exit Latency:** Indicates the length of time this port requires to complete the transition from L1 to L0. The value 010b indicates the range of 2 µs to less than 4 µs. If this field is required to be any value other than the default, BIOS must initialize it accordingly. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	R/WO 010b	**L0s Exit Latency:** Indicates the length of time this port requires to complete the transition from L0s to L0. The value 010b indicates the range of 128 ns to less than 256 ns. If this field is required to be any value other than the default, BIOS must initialize it accordingly. Note: When PCI Express is operating with separate reference clocks, L0s exit latency may be greater than the setting in the L0s Exit Latency Register. Expect longer exit latency then setting in L0s Exit Latency Register. The link may enter Recovery state before reaching L0. System BIOS can program the appropriate Exit Latency and advertised N_FTS value if it detects that the downstream device is not using the common reference clock (indicated in the Slot Clock Configuration bit 12 of the device's Link Status Register)
11:10	RO 11b	**Active State Link PM Support:** L0s and L1 entry supported.
9:4	W/RO 08h	**Max Link Width:** Hardwired to indicate X8. When Force X1 mode is enabled on this PCI Express device, this field reflects X1 (01h).
3:0	RO 1h	**Max Link Speed:** Hardwired to indicate 2.5 Gb/s.

8.1.37 LCTL – Link Control (D1:F0)

PCI Device: 1
Address Offset: B0h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Allows control of PCI Express link.

Bit	Access & Default	Description
15:8		Reserved
7	R/W 0h	**Extended Synch** 0 = Standard Fast Training Sequence (FTS). 1 = Forces extended transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP Ordered Set prior to entering L0, and the transmission of 1024 TS1 ordered sets in the Recovery Rcvr Lock state prior to entering the Recovery Rcvr Cfg state. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication. **NOTE:** This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
6	R/W 0b	**Common Clock Configuration** 0 = Indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1 = Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. **NOTE:** Components use this common clock configuration to report the correct L0s and L1 Exit Latencies.
5	R/W 0b	**Retrain Link** 0 = Normal operation 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).
4	R/W 0b	**Link Disable** 0 = Normal operation 1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0 to 0 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.
3	RO 0b	**Read Completion Boundary (RCB):** Hardwired to 0 to indicate 64 byte.
2		Reserved
1:0	R/W 00b	**Active State PM:** Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Supported 10: Reserved 11: L0s and L1 Entry Supported [

8.1.38 LSTS – Link Status (D1:F0)

PCI Device: 1
Address Offset: B2h
Default Value: 1001h
Access: RO
Size: 16 bits

Indicates PCI Express link status.

Bit	Access & Default	Description
15:13		Reserved
12	RO 1b	**Slot Clock Configuration** 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO 0b	**Link Training:** Indicates that Link training is in progress. Hardware clears this bit once Link training is complete.
10	RO 0b	**Training Error:** This bit is set by hardware upon detection of unsuccessful training of the Link to the L0 Link state.
9:4	RO 00h	**Negotiated Width:** Indicates negotiated link width 00h: Reserved 01h: x1 04h: Reserved 08h: x8 10h: Reserved All other encoding are reserved.
3:0	RO 1h	**Negotiated Speed:** Indicates negotiated link speed. 1h: 2.5 Gb/s All other encodings are reserved.

8.1.39 SLOTCAP – Slot Capabilities (D1:F0)

PCI Device: 1
Address Offset: B4h
Default Value: 00000000h
Access: R/WO
Size: 32 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
31:19	R/WO 0000h	**Physical Slot Number:** Indicates the physical slot number attached to this Port. This field must be initialized by BIOS to a value that assigns a slot number that is globally unique within the chassis.
18:17		Reserved

Bit	Access & Default	Description
16:15	R/WO 00b	**Slot Power Limit Scale:** Specifies the scale used for the Slot Power Limit Value. 00: 1.0x 01: 0.1x 10: 0.01x 11: 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	R/WO 00h	**Slot Power Limit Value:** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	R/WO 0b	**Hot-plug Capable:** Indicates that this slot is capable of supporting Hot-plug operations.
5	R/WO 0b	**Hot-plug Surprise:** Indicates that a device present in this slot might be removed from the system without any prior notification.
4	R/WO 0b	**Power Indicator Present:** Indicates that a Power Indicator is implemented on the chassis for this slot.
3	R/WO 0b	**Attention Indicator Present:** Indicates that an Attention Indicator is implemented on the chassis for this slot.
2:1		Reserved
0	R/WO 0b	**Attention Button Present:** Indicates that an Attention Button is implemented on the chassis for this slot. The Attention Button allows the user to request hot-plug operations.

8.1.40 SLOTCTL – Slot Control (D1:F0)

PCI Device: 1
Address Offset: B8h
Default Value: 01C0h
Access: R/W
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
15:10		Reserved
9:8	R/W 01b	**Power Indicator Control:** Reads to this register return the current state of the Power Indicator. Writes to this register set the Power Indicator and cause the port to send the appropriate POWER_INDICATOR_* messages. 00: Reserved 01: On 10: Blink 11: Off

Bit	Access & Default	Description
7:6	R/W 11b	**Attention Indicator Control:** Reads to this register return the current state of the Attention Indicator. Writes to this register set the Attention Indicator and cause the port to send the appropriate ATTENTION_INDICATOR_* messages. 00: Reserved 01: On 10: Blink 11: Off
5	R/W 0b	**Hot plug Interrupt Enable:** When set enables generation of hot plug interrupt on enabled hot plug events.
4	R/W 0b	**Command Completed Interrupt Enable:** When set enables the generation of hot plug interrupt when the Hot plug controller completes a command.
3	R/W 0b	**Presence Detect Changed Enable:** When set enables the generation of hot plug interrupt or wake message on a presence detect changed event.
2:1		Reserved
0	R/W 0b	**Attention Button Pressed Enable:** When set enables the generation of hot plug interrupt or wake message on an attention button pressed event.

8.1.41 SLOTSTS – Slot Status (D1:F0)

PCI Device: 1
Address Offset: BAh
Default Value: 0000h
Access: RO, R/W/C
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
15:7		Reserved
6	RO Xb	**Presence Detect State:** Indicates the presence of a card in the slot. 0 = Slot Empty 1 = Card Present in slot.
5		Reserved
4	R/WC 0b	**Command Completed:** Set when the hot plug controller completes an issued command.
3	R/WC 0b	**Presence Detect Changed:** Set when a Presence Detect change is detected. This corresponds to an edge on the signal that corresponds to bit 6 of this register (Presence Detect State).
2:1		Reserved
0	R/WC 0b	**Attention Button Pressed:** Set when the Attention Button is pressed.

8.1.42 RCTL – Root Control (D1:F0)

PCI Device: 1
Address Offset: BCh
Default Value: 0000h
Access: R/W
Size: 16 bits

Allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access & Default	Description
15:4		Reserved
3	R/W 0b	**PME Interrupt Enable** 0 = No interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	R/W 0b	**System Error on Fatal Error Enable:** Controls the Root Complex's response to fatal errors. 0 = No SERR generated on receipt of fatal error. 1 = Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	R/W 0b	**System Error on Non-Fatal Uncorrectable Error Enable:** Controls the Root Complex's response to non-fatal errors. 0 = No SERR generated on receipt of non-fatal error. 1 = Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	R/W 0b	**System Error on Correctable Error Enable:** Controls the Root Complex's response to correctable errors. 0 = No SERR generated on receipt of correctable error. 1 = Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

8.1.43 RSTS – Root Status (D1:F0)

PCI Device: 1
Address Offset: C0h
Default Value: 00000000h
Access: RO, R/W/C
Size: 32 bits

Provides information about PCI Express Root Complex specific parameters.

Bit	Access & Default	Description
31:18		Reserved
17	RO 0b	**PME Pending:** Indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	R/W/C 0b	**PME Status:** Indicates that the requestor ID indicated in the PME Requestor ID field asserted PME. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO 0000h	**PME Requestor ID:** Indicates the PCI requestor ID of the last PME requestor.

8.1.44 PEGLC – PCI Express Legacy Control

PCI Device: 1
Address Offset: ECh
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

PCI Device: 1
Address Offset: ECh
Size: 32 bits

Controls functionality that is needed by Legacy (non-PCI Express aware) OSes during run time.

Bit	Access & Default	Description
31:3	RO 00000000h	Reserved
2	R/W 0b	**PME GPE Enable** (PMEGPE) 0 = Do not generate GPE PME message when PME is received. 1 = Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the MCH to support PMEs on the PCI Express* port under legacy OSes.

Bit	Access & Default	Description
1	R/W 0b	**Hot-Plug GPE Enable** (HPGPE) 0 = Do not generate GPE Hot-Plug message when Hot-Plug event is received. 1 = Generate a GPE Hot-Plug message when Hot-Plug Event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the MCH to support Hot-Plug on the PCI Express port under legacy OSes.
0	R/W 0b	**General Message GPE Enable** (GENGPE) 0 = Do not forward received GPE assert/deassert messages. 1 = Forward received GPE assert/deassert messages. These general GPE message can be received via the PCI Express port from an external Intel® device (i.e. PXH) and will be subsequently forwarded to the ICH (via Assert_GPE and Deassert_GPE messages on DMI). For example, a PXH might send this message if a PCI Express device is hot plugged into a PXH downstream port.

8.1.45 VCECH – Virtual Channel Enhanced Capability Header (D1:F0)

PCI Device: 1
Address Offset: 100h
Default Value: 14010002h
Access: RO
Size: 32 bits

Indicates PCI Express device Virtual Channel capabilities.

Note that extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access & Default	Description
31:20	RO 140h	**Pointer to Next Capability:** The Link Declaration Capability is the next in the PCI Express* extended capabilities list.
19:16	RO 1h	**PCI Express Virtual Channel Capability Version:** Hardwired to 1 to indicate compliances with the 1.0a version of the PCI Express specification.
15:0	RO 0002h	**Extended Capability ID:** Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

8.1.46 PVCCAP1 – Port VC Capability Register 1 (D1:F0)

PCI Device: 1
Address Offset: 104h
Default Value: 00000001h
Access: RO, R/WO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7		Reserved
6:4	RO 000b	**Low Priority Extended VC Count:** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3		Reserved
2:0	R/WO 001b	**Extended VC Count:** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

8.1.47 PVCCAP2 – Port VC Capability Register 2 (D1:F0)

PCI Device: 1
Address Offset: 108h
Default Value: 00000001h
Access: RO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset:** Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8		Reserved
7:0	RO 01h	**VC Arbitration Capability:** Indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority, VC0 is the lowest priority.

8.1.48 PVCCTL – Port VC Control (D1:F0)

PCI Device: 1
Address Offset: 10Ch
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:4		Reserved
3:1	R/W 000b	**VC Arbitration Select:** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 001b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field can not be modified when more than one VC in the LPVC group is enabled.
0		Reserved

8.1.49 VC0RCAP – VC0 Resource Capability (D1:F0)

PCI Device: 1
Address Offset: 110h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 0b	**Reject Snoop Transactions** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		Reserved

8.1.50 VC0RCTL – VC0 Resource Control (D1:F0)

PCI Device: 1
Address Offset: 114h
Default Value: 8000007Fh
Access: RO, R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**VC0 Enable:** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27		Reserved
26:24	RO 000b	**VC0 ID:** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:8		Reserved
7:1	R/W 7Fh	**TC/VC0 Map:** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 1b	**TC0/VC0 Map:** Traffic Class 0 is always routed to VC0.

8.1.51 VC0RSTS – VC0 Resource Status (D1:F0)

PCI Device: 1
Address Offset: 11Ah
Default Value: 0000h
Access: RO
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 0b	**VC0 Negotiation Pending** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as wherever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0		Reserved

8.1.52 VC1RCAP – VC1 Resource Capability (D1:F0)

PCI Device: 1
Address Offset: 11Ch
Default Value: 00008000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 1b	**Reject Snoop Transactions** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		Reserved

8.1.53 VC1RCTL – VC1 Resource Control (D1:F0)

PCI Device: 1
Address Offset: 120h
Default Value: 01000000h
Access: RO, R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0b	**VC1 Enable** 0 = Virtual Channel is disabled. 1 = Virtual Channel is enabled. See exceptions in note below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express* port); a 0 read from this bit indicates that the Virtual Channel is currently disabled. **NOTES:** 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
30:27		Reserved
26:24	R/W 001b	**VC1 ID:** Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field cannot be modified when the VC is already enabled.
23:8		Reserved

Bit	Access & Default	Description
7:1	R/W 00h	**TC/VC1 Map:** Indicate the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 0b TC0/VC1 Map	Traffic Class 0 is always routed to VC0.

8.1.54 VC1RSTS – VC1 Resource Status (D1:F0)

PCI Device: 1
Address Offset: 126h
Default Value: 0000h
Access: RO
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 0b	**VC1 Negotiation Pending** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as wherever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0		Reserved

8.1.55 RCLDECH – Root Complex Link Declaration Enhanced Capability Header (D1:F0)

PCI Device: 1
Address Offset: 140h
Default Value: 000100005h
Access: RO
Size: 32 bits

This capability declares links from this element to other elements of the root complex component to which it belongs. See PCI Express specification for link/topology declaration requirements.

Bit	Access & Default	Description
31:20	RO 000h	**Pointer to Next Capability:** This is the last capability in the PCI Express* extended capabilities list.
19:16	RO 1h	**Link Declaration Capability Version:** Hardwired to 1 to indicate compliances with the 1.0 version of the PCI Express specification.
15:0	RO 0005h	**Extended Capability ID:** Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

Note: See corresponding Egress Port Link Declaration Capability registers for diagram of Link Declaration Topology.

8.1.56 ESD – Element Self Description (D1:F0)

PCI Device: 1
Address Offset: 144h
Default Value: 02000100h
Access: RO, R/WO
Size: 32 bits

Provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number:** Specifies the port number associated with this element with respect to the component that contains this element. The egress port of the component to provide arbitration to this Root Complex Element utilizes this port number value.
23:16	R/WO 00h	**Component ID:** Identifies the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 01h	**Number of Link Entries:** Indicates the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as we don't report any peer-to-peer capabilities in our topology).
7:4		Reserved
3:0	RO 0h	**Element Type:** Indicates the type of the Root Complex Element. Value of 0h represents a root port.

8.1.57 LE1D – Link Entry 1 Description (D1:F0)

PCI Device: 1
Address Offset: 150h
Default Value: 00000000h
Access: RO, R/WO
Size: 32 bits

First part of a Link Entry, which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 00h	**Target Port Number:** Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 0b	**Link Type:** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

8.1.58 LE1A – Link Entry 1 Address (D1:F0)

PCI Device: 1
Address Offset: 158h
Default Value: 0000000000000000h
Access: R/WO
Size: 64 bits

Second part of a Link Entry, which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32		Reserved
31:12	R/WO 00000h	**Link Address:** Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0		Reserved

8.1.59 PEGSSTS – PCI Express Sequence Status (D1:F0)

PCI Device: 1
Address Offset: 218h
Default Value: 0000000000000FFFh
Access: RO
Size: 64 bits

PCI Express status reporting that is required by the PCI Express specification.

Bit	Access & Default	Description
63:60		Reserved
59:48	RO 000h	**Next Retry Buffer Entry Sequence Number:** Value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next TLP to be transmitted onto the Link for the first time.
47:44		Reserved
43:32	RO 000h	**Next Packet Sequence Number:** Packet sequence number to be applied to the next TLP to be transmitted or retransmitted onto the Link.
31:28		**Reserved**
27:16	RO 000h	**Next Receive Sequence Number:** This is the sequence number associated with the TLP that is expected to be received next.
15:12		Reserved
11:0	RO FFFh	**Last Acknowledged Sequence Number:** This is the sequence number associated with the last acknowledged TLP.

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9 Device 2 Internal Graphics Registers Summary (D2:F0)

Device 2 contains registers for the internal graphics functions. The table below lists the PCI configuration registers in order of ascending offset address.

Function 0 can be VGA compatible or not, this is selected through bit 1 of GGC register (Device 0, offset 52h).

Note: The following sections describe Device 2 PCI configuration registers only.

9.1 Device 2 Function 0 Configuration Register Details (D2:F0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00-01h	VID2	Vendor Identification	8086h	RO
02-03h	DID2	Device Identification	258Ah	RO
04-05h	PCICMD2	PCI Command	0000h	RO, R/W
06-07h	PCISTS2	PCI Status	0090h	RO
08h	RID2	Revision Identification	00h	RO
09-0Bh	CC	Class Code	030000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type	80h	RO
0Fh	—	Reserved	—	—
10-13h	MMADR	Memory Mapped Range Address	00000000h	RO, R/W
14-17h	IOBAR	I/O Base Address	00000001h	RO, R/W
18-1Bh	GMADR	Graphics Memory Range Address	00000008h	RO, R/W/L
1C-1Fh	GTTADR	Graphics Translation Table Range Address	00000000h	RO, R/W
20-2Bh	—	Reserved	—	—
2C-2Dh	SVID2	Subsystem Vendor Identification	0000h	R/WO
2E-2Fh	SID2	Subsystem Identification	0000h	R/WO
30-33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	D0h	RO
35-3Bh	—	Reserved	—	—
3Ch	INTRLINE	Interrupt Line	00h	RO
3Dh	INTRPIN	Interrupt Pin	01h	RO
3Eh	MINGNT	Minimum Grant	00h	RO

Address Offset	Register Symbol	Register Name	Default Value	Access
3Fh	MAXLAT	Maximum Latency	00h	RO
40-CFh	—	Reserved	—	—
D0-D1h	PMCAPID	Power Management Capabilities ID	0001h	RO
D2-D3h	PMCAP	Power Management Capabilities	0022h	RO
D4-D5h	PMCS	Power Management Control/Status	0000h	RO, R/W
D6-FFh	—	Reserved	—	—

9.1.1 VID2 – Vendor Identification (D2:F0)

PCI Device: 2
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

9.1.2 DID2 – Device Identification (D2:F0)

PCI Device: 2
Address Offset: 02h
Default Value: 258Ah
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 258Ah	**Device Identification Number (DID):** This is a 16-bit value assigned to the MCH Graphic device

9.1.3 PCICMD2 – PCI Command (D2:F0)

PCI Device: 2
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This 16 bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:11		Reserved
10	R/W 0b	**Interrupt Disable:** This bit disables the device from asserting INTx#. 0 = Enable the assertion of this device's INTx# signal. 1 = Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	RO 0b	**Fast Back-to-Back (FB2B)**: Not Implemented. Hardwired to 0.
8	RO 0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO 0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0b	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W 0b	**Bus Master Enable (BME)** 0 = Disable IGD bus mastering. 1 = Enable the IGD to function as a PCI compliant master.
1	R/W 0b	**Memory Access Enable (MAE)**: This bit controls the IGD's response to memory space accesses. 0 = Disable. 1 = Enable.
0	R/W 0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0 = Disable. 1 = Enable.

9.1.4 PCISTS2 – PCI Status (D2:F0)

PCI Device: 2
Address Offset: 06h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Since the IGD does not detect parity; this bit is always hardwired to 0.
14	RO 0b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO 0b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO 0b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00b	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to “00”.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0b	**User Defined Format (UDF).** Hardwired to 0.
5	RO 0b	**66 MHz PCI Capable (66C).** N/A – Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function’s PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO 0b	**Interrupt Status:** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
2:0		Reserved

9.1.5 RID2 – Revision Identification (D2:F0)

PCI Device: 2
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number for Device 2 Functions 0.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the MCH. For the A-0 Stepping, this value is 00h.

9.1.6 CC – Class Code (D2:F0)

PCI Device: 2
Address Offset: 09h
Default Value: 030000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the MCH. This code has the value 03h, indicating a Display Controller.
15:8	RO 00h	**Sub-Class Code (SUBCC):** Value will be determined based on Device 0 GGC register, bit 1. 00h: VGA compatible 80h: Non VGA
7:0	RO 00h	**Programming Interface (PI):** 00h: Hardwired as a Display controller.

9.1.7 CLS – Cache Line Size (D2:F0)

PCI Device: 2
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** This field is hardwired to 0's. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

9.1.8 MLT2 – Master Latency Timer (D2:F0)

PCI Device: 2
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer Count Value:** Hardwired to 0's.

9.1.9 HDR2 – Header Type (D2:F0)

PCI Device: 2
Address Offset: 0Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access & Default	Description
7	RO 1b	**Multi Function Status (MFunc):** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN [4]. If Device 0 DEVEN [4] is set, the Mfunc bit is also set.
6:0	RO 00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

9.1.10 MMADR – Memory Mapped Range Address (D2:F0)

PCI Device: 2
Address Offset: 10h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].

Bit	Access & Default	Description
31:19	R/W 0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:19].
18:4	RO 0000h	**Address Mask:** Hardwired to 0's to indicate 512 KB address range.
3	RO 0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO 00b	**Memory Type:** Hardwired to 0's to indicate 32-bit address.
0	RO 0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

9.1.11 IOBAR – I/O Base Address (D2:F0)

PCI Device: 2
Address Offset: 14h
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This register provides the Base offset of the I/O registers within Device 2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16 bit I/O Address Space. Bits 2:1 are fixed and return zero, bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded.

Access to the 8Bs of I/O space is allowed in PM state D0 when I/O Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device 2 is turned off.

Note: Access to this IO BAR is independent of VGA functionality within Device 2.

If accesses to this I/O bar are allowed then the MCH claims all 8, 16 or 32 bit I/O cycles from the processor that falls within the 8B claimed.

Bit	Access & Default	Description
31:16		Reserved
15:3	R/W 0000h	**I/O Base Address:** Set by the OS, these bits correspond to address signals [15:3].

Bit	Access & Default	Description
2:1	RO 00b	**Memory Type:** Hardwired to 0's to indicate 32-bit address.
0	RO 1b	**Memory I/O Space:** Hardwired to "1" to indicate I/O space.

9.1.12 GMADR – Graphics Memory Range Address (D2:F0)

PCI Device: 2
Address Offset: 18h
Default Value: 00000008h
Access: RO, R/W/L
Size: 16 bits

IGD graphics memory base address is specified in this register.

Bit	Access & Default	Description
31:28	R/W 0h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:28].
27:4	RO 000000h	**Address Mask:** Hardwired to 0's to indicate at least 256MB address range
3	RO 1b	**Prefetchable Memory:** Hardwired to 1 to enable prefetching
2:1	RO 00b	**Memory Type:** Hardwired to 0 to indicate 32-bit address.
0	RO 0b	**Memory I/O Space:** Hardwired to 0 to indicate memory space.

9.1.13 GTTADR – Graphics Translation Table Range Address (D2:F0)

PCI Device: 2
Address Offset: 1Ch
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for Graphics Translation Table Range. The allocation is for 256KB and the base address is defined by bits [31:18].

Bit	Access & Default	Description
31:18	R/W 0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:18].
17:4	RO 0000h	**Address Mask:** Hardwired to 0's to indicate 256KB address range.
3	RO 0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.

Bit	Access & Default	Description
2:1	RO 00b	**Memory Type:** Hardwired to 0's to indicate 32-bit address.
0	RO 0b	**Memory I/O Space:** Hardwired to 0 to indicate memory space.

9.1.14 SVID2 – Subsystem Vendor Identification (D2:F0)

PCI Device: 2
Address Offset: 2Ch
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID:** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read-Only. This register can only be cleared by a Reset.

9.1.15 SID2 – Subsystem Identification (D2:F0)

PCI Device: 2
Address Offset: 2Eh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Identification:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

9.1.16 ROMADR – Video BIOS ROM Base Address (D2:F0)

PCI Device: 2
Address Offset: 30h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM; therefore this register is hardwired to 0's.

Bit	Access & Default	Description
31:18	RO 0000h	**M Base Address:** Hardwired to 0's.

17:11	RO 00h	**Address Mask:** Hardwired to 0's to indicate 256KB address range.
10:1		Reserved
0	RO 0b	**ROM BIOS Enable** 0 = ROM not accessible.

9.1.17 CAPPOINT – Capabilities Pointer (D2:F0)

PCI Device: 2
Address Offset: 34h
Default Value: D0h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO D0h	**Capabilities Pointer Value:** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the Power Management Capabilities ID registers at address D0h.

9.1.18 INTRLINE – Interrupt Line (D2:F0)

PCI Device: 2
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00h	**Interrupt Connection:** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that the device's interrupt pin is connected to.

9.1.19 INTRPIN – Interrupt Pin (D2:F0)

PCI Device: 2
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin:** As a device which only has interrupts associated with a single function, the IGD specifies INTA# as its interrupt pin. 01h: INTA#

9.1.20 MINGNT – Minimum Grant (D2:F0)

PCI Device: 2
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Minimum Grant Value:** The IGD does not burst as a PCI compliant master.

9.1.21 MAXLAT – Maximum Latency (D2:F0)

PCI Device: 2
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Maximum Latency Value:** The IGD has no specific requirements for how often it needs to access the PCI bus.

9.1.22 PMCAPID – Power Management Capabilities ID (D2:F0)

PCI Device: 2
Address Offset: D0h
Default Value: 0001h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	**NEXT_PTR:** This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO 01h	**CAP_ID:** SIG defines this ID is 01h for power management.

9.1.23 PMCAP – Power Management Capabilities (D2:F0)

PCI Device: 2
Address Offset: D2h
Default Value: 0022h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00h	**PME Support:** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO 0b	**D2:** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO 0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6		Reserved
5	RO 1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO 0b	**Auxiliary Power Source:** Hardwired to 0.
3	RO 0b	**PME Clock:** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO 010b	**Version:** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with Rev. 1.1 of the *PCI Power Management Interface Specification*.

9.1.24 PMCS – Power Management Control/Status (D2:F0)

PCI Device: 2
Address Offset: D4h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**PME_Status:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:9		Reserved
8	RO 0b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.

Bit	Access & Default	Description
7:2		**Reserved**
1:0	R/W 00b	**Power State:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in Section 11.5, “Power Management” on page 11-178 **Bits [1:0]Power state** 00 D0 Default 01 D1 Not Supported 10 D2 Not Supported 11 D3

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10 System Address Map

The MCH supports 4 GB of addressable memory space and 64 KB+3 bytes of addressable I/O space. There is a programmable memory address space under the 1 MB region that is divided into regions which can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained near the end of this section.

Addressing of memory ranges larger than 4 GB is NOT supported. The HREQ[4:3] FSB pins are decoded to determine whether the access is above or below 4GB.

The MCH does not support the PCI Dual Address Cycle Mechanism, PCI Express 64-bit prefetchable memory transactions, or any other addressing mechanism that allows addressing of greater than 4 GB on either the DMI Interface or PCI Express interface. The MCH does not limit DRAM space in hardware. There is no hardware lock to stop someone from inserting more memory than is addressable.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI Interface. The exception to this rule is VGA ranges, which may be mapped to PCI Express, DMI, or the integrated graphics. In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI Interface/PCI, while cycle descriptions referencing PCI Express or integrated graphics are related to the PCI Express bus. The MCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable Dram). The TOLUD register is set to the appropriate value by BIOS.

The Address Map includes a number of programmable ranges:

Device 0:

- EPBAR – Egress port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4KB window)
- MCHBAR – Memory mapped range for internal MCH registers. For example, memory buffer register controls. (16KB window)
- PCIEXBAR – Flat memory-mapped address space to access device configuration registers. This mechanism can be used to access PCI configuration space (0-FFh) and Extended configuration space (100h-FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (256 MB window).
- DMIBAR – This window is used to access registers associated with the MCH/ICH Serial Interconnect (DMI) register memory range. (4KB window)
- IFPBAR – Any write to this window will trigger a flush of the MCH's Global Write Buffer to let software guarantee coherency between writes from an isochronous agent and writes from the processor (4KB window).
- GGC – MCH Graphics Control register. Used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes. (0-64MB options).

Device 1:

- MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
- PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.
- IOBASE1/IOLIMIT1 – PCI Express port I/O access window.

Device 2:

- MMADR – IGD registers and internal graphics instruction port. (512KB window)
- IOBAR – I/O access window for internal graphics. Through this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed. Note that this allows accessing the same registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTTADR table.
- GMADR – Internal graphics translation window. (256MB window)
- GTTADR – Internal graphics translation table location. (256KB window). Note that the PGTBL_CTL register (MMIO 2020) indicates the physical address base which is 4KB aligned.

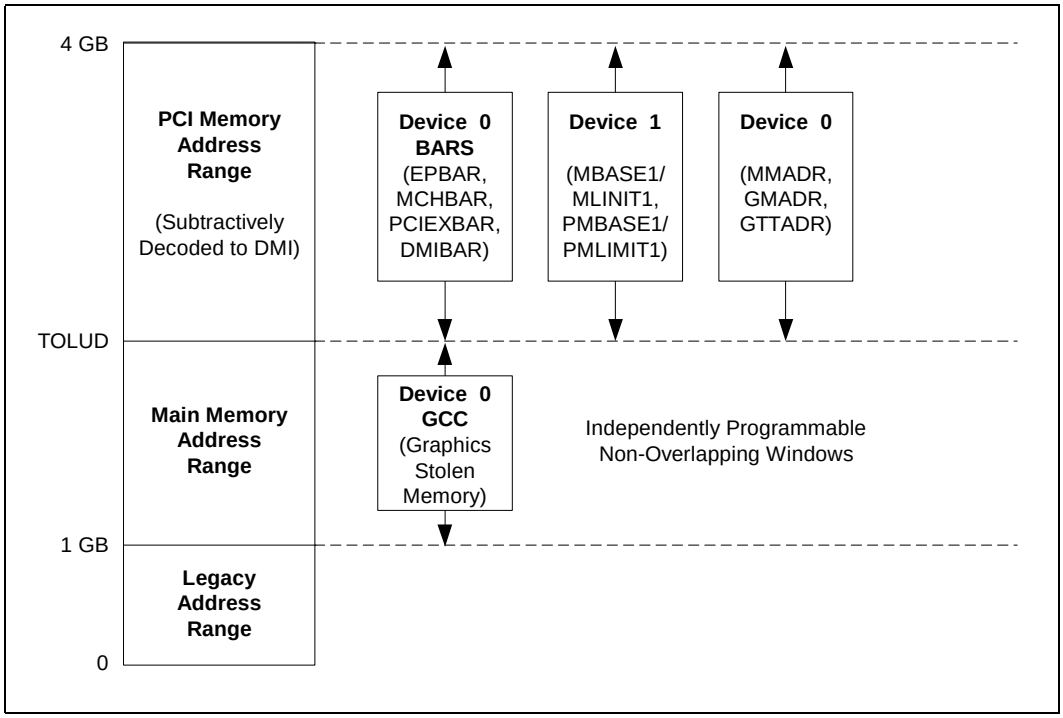
The rules for the above programmable ranges are:

1. ALL of these ranges MUST be unique and NON-OVERLAPPING. **It is the BIOS or system designer's responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.**
2. In the case of overlapping ranges with memory, the memory decode will be given priority.
3. There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
4. Accesses to overlapped ranges may produce indeterminate results.
5. The only peer-to-peer cycles allowed below the top of memory (register TOLUD) are DMI to PCI Express VGA ranges writes.

Note: That peer to peer cycles to the Internal Graphics VGA range are not supported.

Figure 10-1 Represents system memory address map in a simplified form.

Figure 10-1. Intel® E7221 System Address Ranges



10.1 Legacy Address Range

This area is divided into the following address regions:

- 0 – 640 KB – DOS Area
- 640 – 768 KB – Legacy Video Buffer Area
- 768 – 896 KB in 16KB sections (total of 8 sections) – Expansion Area
- 896 – 960 KB in 16KB sections (total of 4 sections) – Extended System BIOS Area
- 960 KB – 1 MB Memory – System BIOS Area

10.1.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the MCH.

10.1.2 Legacy Video Range (A_0000h – B_FFFFh)

The legacy 128K VGA memory range, frame buffer, (000A_0000h - 000B_FFFFh) can be mapped to Device 2, to PCI Express, and/or to DMI. The appropriate mapping depends on which devices are enable and programming of the VGA steering bits. Based on the VGA steering bits, priority of VGA mapping is constant. The MCH always decodes internally mapped devices first. Internal to the MCH, decode precedence is always given to the Device 2. The MCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configuration bits (VGA) Enable & MDAP). This region is also the default for SMM space.

Compatible SMRAM Address Range (A_0000h -b_ffffh)
When compatible SMM space is enable, SMM-mode CPU accesses to this range are routed to physical system DRAM at 000A 0000h - 000B FFFFh. Non-SMM-mode CPU accesses to this range are consider to be the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed. and are considered to be to the Video Buffer Area if Device 2 is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as Peer cycles, and will master abort on PCI if no external VGA device claims them.

Monochrome Adapter (MDA) Range (B_0000h - B_7FFFh)
Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forward to Device 2, PCI Express, or DMI (depending on configuration bits). Since the monochrome adapter may be mapped to any one of these devices, the MCH must decode cycles in the MDA range (000B_0000h - 000B_7FFFh) and forward either to Device 2, PCI Express nd/or DMI. This additions to the memory range B0000h to B7FFFh, the MCH decodes I/O cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh and forwards them to either Device 2, PCI Express and/or DMI.

10.1.3 Expansion Area (C_0000h – D_FFFFh)

This 128 Kbytes ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight 16 Kbytes segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through MCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Figure 10-2. DOS Legacy Address Range

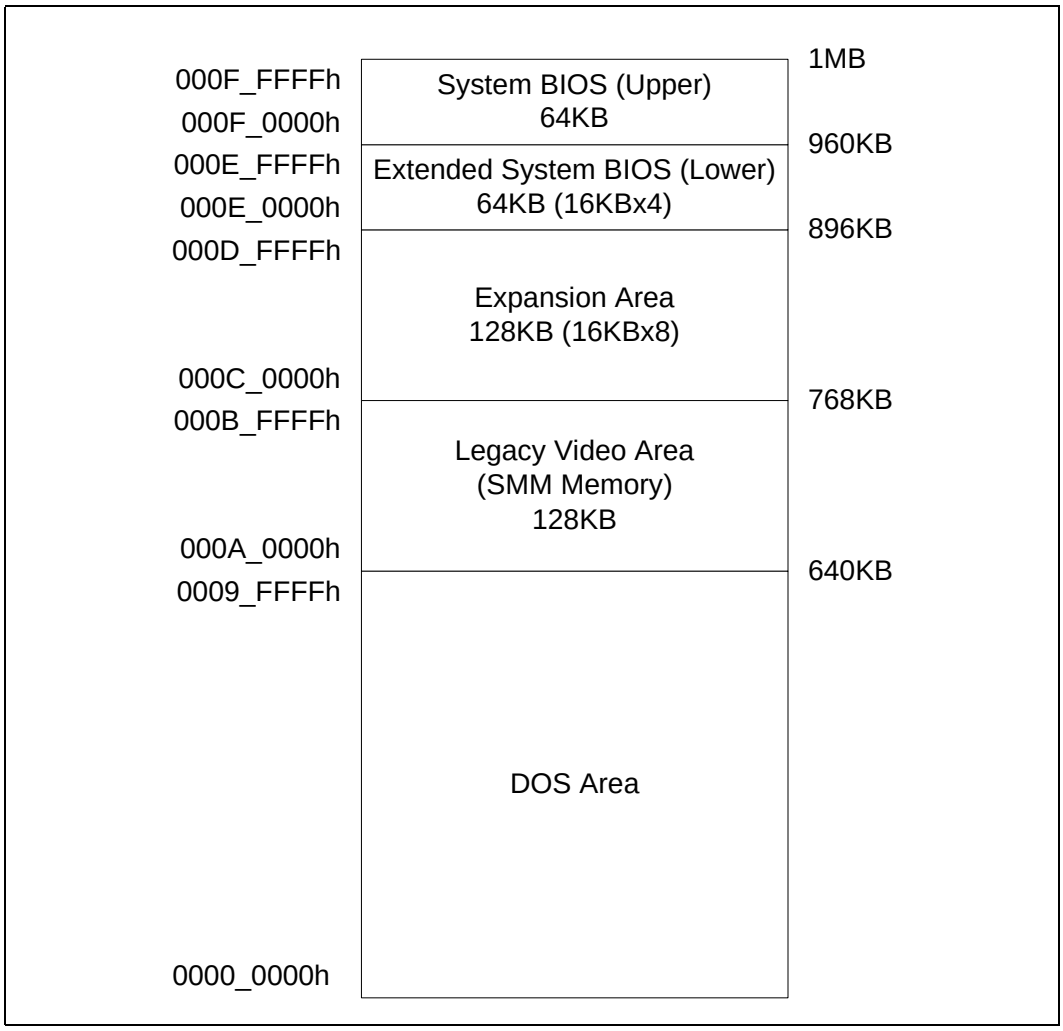


Table 10-1. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000H – 0C3FFFH	WE RE	Add-on BIOS
0C4000H – 0C7FFFH	WE RE	Add-on BIOS
0C8000H – 0CBFFFH	WE RE	Add-on BIOS
0CC000H – 0CFFFFH	WE RE	Add-on BIOS
0D0000H – 0D3FFFH	WE RE	Add-on BIOS
0D4000H – 0D7FFFH	WE RE	Add-on BIOS
0D8000H – 0DBFFFH	WE RE	Add-on BIOS
0DC000H – 0DFFFFH	WE RE	Add-on BIOS

10.1.4 Extended System BIOS Area (E_0000h – E_FFFFh)

This 64 Kbytes area (000E_0000h – 000E_FFFFh) is divided into four 16 Kbytes segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI Interface. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 10-2. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000H – 0E3FFFH	WE RE	BIOS Extension
0E4000H – 0E7FFFH	WE RE	BIOS Extension
0E8000H – 0EBFFFH	WE RE	BIOS Extension
0EC000H – 0EFFFFH	WE RE	BIOS Extension

10.1.5 System BIOS Area (F_0000h – F_FFFFh)

This area is a single 64 Kbytes segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled, and cycles are forwarded to DMI Interface. By manipulating the Read/Write attributes, the MCH can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 10-3. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000H – 0FFFFFH	WE RE	BIOS Area

10.1.6 PAM (Programmable Attribute Map) Memory Area Details

The 13 sections from 768 KB to 1MB comprise what is also known as the PAM Memory Area.

The MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there will normally not be IWB cycles targeting DMI.

However, DMI becomes the default target for processor and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RC it is possible to get IWB cycles targeting DMI. This may occur for processor originated cycles and for DMI originated cycles to disabled PAM regions.

Warning: For example, say that a particular PAM region is set for “Read Disabled” and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is “Read Disabled” the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the MCH to hang.

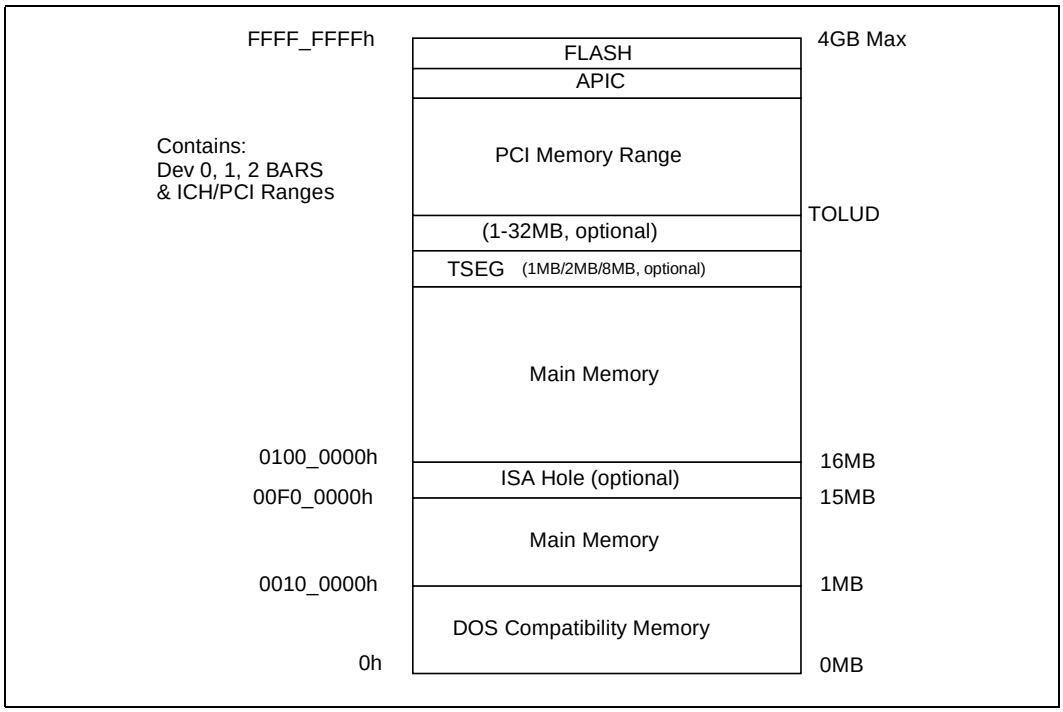
10.2 Main Memory Address Range (1MB to TOLUD)

This address range extends from 1 MB to the top of physical memory that is permitted to be accessible by the MCH (as programmed in the TOLUD register). All accesses to addresses within this range will be forwarded by the MCH to the DRAM unless they falls into the optional TSEG, or optional ISA Hole, or optional IGD stolen VGA memory.

The MCH provides a maximum DRAM address decode space of 4GB. The MCH does not remap APIC or PCI Express memory space. This means that as the amount of physical memory populated in the system reaches 4GB, there will be physical memory that exists yet is non-addressable and therefore unusable by the system.

Note: The MCH does not limit DRAM address space in hardware.

Figure 10-3. Main Memory Address Range



10.2.1 ISA Hole (15 – 16 MB)

A hole can be created at 15MB-16MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI Interface. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15MB-16MB hole is an optionally enabled ISA hole.

Video accelerators originally used this hole. It is also used by validation and customer SV teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15-16 MB window.

10.2.2 TSEG

TSEG is optionally 1MB, 2MB, or 8MB in size. TSEG is below integrated graphics stolen memory, which is at the top of physical memory. SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-processor originated accesses are not allowed to SMM space. PCI Express, and DMI originated cycle to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses. Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled, the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1MB, 2MB, or 8MB.

10.2.3 Pre-Allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions**. The following table details the location and attributes of the regions. Enabling/Disabling these ranges are described in the MCH Control Register Device 0 (GCC).

Table 10-4. Pre-Allocated Memory Example for 64 MB DRAM and 1 MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03DF_FFFFh	R/W	Available System Memory 62 MB
03E0_0000h – 03EF_FFFFh	SMM Mode Only – Processor Reads	TSEG Address Range & Pre-allocated Memory
03F0_0000h - 03FF_FFFFh	R/W	Pre-allocated Graphics VGA memory. 1MB (or 4/8/16/32/64 MB) with Integrated Graphics is enabled.

10.3 PCI Memory Address Range (TOLUD – 4GB)

This address range, from the top of physical memory to 4GB (top of addressable memory space supported by the MCH) is normally mapped via the DMI Interface to PCI.

Exceptions to this mapping include the “bar” memory mapped regions. This includes:

- EPBAR, MCHBAR and DMIBAR. With PCI Express port, there are two exceptions to this rule.
  a. Addresses decoded to the PCI Express Memory Window defined by the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers are mapped to PCI Express.
  b. Addresses decoded to PCI Express Configuration Space are mapped based on Bus, Device, and Function number. (PCIEXBAR range).

10.3.1 APIC Configuration Space (FEC0_0000h – FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the ICH6 portion of the chip-set, but may also exist as stand-alone components.

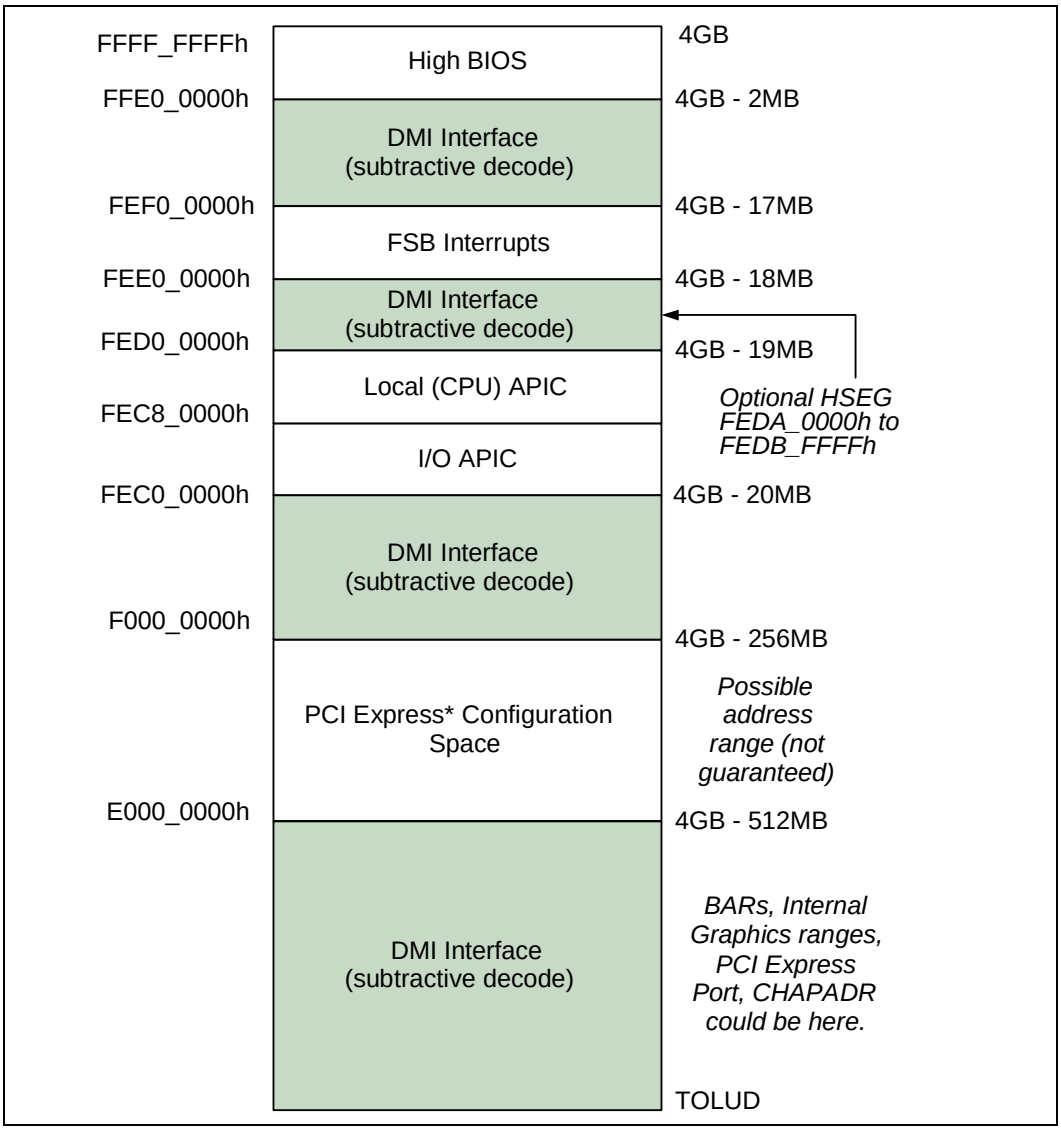
The I/O APIC space are used to communicate with I/O APIC interrupt controller that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor caches to the default I/O APIC region (FEC0_0000h to FEC7_FFFFh) are always forwarded to DMI.

The third exception to the mapping rule occurs in an integrated graphics configuration:

- Addresses decoded to the Graphics Memory Range. (GMADR range)
- Addresses decoded to the Memory Mapped range of the Memory Mapped Range of the Integrated Graphics Device (MMADR range). There is a MMADR range for Device 2 function 0.

The exception listed above for Internal Graphics and the PCI Express ports MUST NOT overlap with APIC configuration, FSB Interrupt Space and High BIOS Address Range.

Figure 10-4. PCI Memory Address Range



10.3.2 HSEG (FEDA_0000h –FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM Memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A_0000h – 000B_FFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode Write Back cycles which are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All cache line writes with WB attribute or Implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

10.3.3 FSB Interrupt Memory Space (FEE0_0000 – FEEF_FFFF)

The FSB Interrupt memory space is the address used to deliver interrupts to the FSB. Any device on PCI Express or DMI may issue a Memory Write to 0FEEx_xxxxh. The MCH will forward this Memory Write along with the data to the FSB as an Interrupt Message Transaction. The MCH terminates the FSB transaction by providing the response and asserting HTRDY#. This Memory Write cycle does not go to DRAM.

10.3.4 High BIOS Area

The top 2MB (FFE0_0000h -FFFF_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to the DMI Interface so that the upper subset of this region aliases to 16MB-256KB range. The actual address space required for the BIOS is less than 2MB but the minimum processor MTRR range for this region is 2MB so that full 2MB must be considered.

10.3.5 PCI Express Configuration Address Space

There is a Device 0 register, PCIEXBAR, that defines the base address for the 256 MB block of addresses below top of addressable memory (currently 4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. This range will be aligned to a 256 MB boundary. BIOS must assign this address range such that it will not conflict with any other address ranges.

10.3.6 PCI Express

The MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.
- The second range is controlled via the Prefetchable Memory Base (PMBASE) and Prefetchable Memory Limit (PMLIMIT) registers.

The MCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

$$\text{Memory\_Base\_Address} \le \text{Address} \le \text{Memory\_Limit\_Address}$$
$$\text{Prefetchable\_Memory\_Base\_Address} \le \text{Address} \le \text{Prefetchable\_Memory\_Limit\_Address}$$

It is essential to support a separate Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note: The MCH Device 1 memory range registers described above are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the Device 1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

10.3.7 AGP DRAM Graphics Aperture

Unlike AGP, PCI Express has no concept of aperture for PCI Express devices. As a result, there is no need to translate addresses from PCI Express. Therefore, the MCH has no APBASE and APSIZE registers.

10.3.8 Graphics Memory Address Ranges

The MCH can be programmed to direct memory access to the integrated graphics device when addresses are within any of the three ranges specified via registers in MCH's Device 2 configuration space.

1. The Memory Map base Register (MMADR) is used to access graphics control registers.
2. The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated via the graphics translation table.
3. The Graphics Translation Table Base Register (GTTADR) is used to access the translation table.

Normally these ranges will reside above the TOP-of-Main_DRAM and below High BIOS and APIC address ranges. The

10.3.9 Graphics Register Ranges

This section provides a high-level register map (register groupings per function) for the integrated graphics. The memory and I/O maps for the graphics registers are shown below, except PCI Configuration registers. The VGA and Extended VGA registers can be accessed via standard VGA I/O locations as well as via memory-mapped locations. In addition, the memory map contains allocation ranges for various functions. The same memory space can be accessed via Dwords accesses to IOBAR. Through the IOBAR, I/O registers MMIO_index and MMIO_data are written.

- VGA and Extended VGA Control Registers (00000h-00FFFh)
  These registers are located in both I/O space and memory space. The VGA and Extended VGA registers contain the following register sets: General Control/Status, Sequencer (SRxx), Graphics Controller (GRxx), Attribute Controller (ARxx), VGA Color Palette, and CRT Controller (CRxx) registers. The registers within a set are accessed using an indirect addressing mechanism as described at the beginning of each section. Note that some of the register description sections have additional operational information at the beginning of the section.
- Instruction, Memory, and Interrupt Control Registers (01000h-02FFFh)

The Instruction and Interrupt Control registers are located in main memory space.

10.3.10 I/O Mapped Access to Device 2 MMIO Space

If Device 2 is enabled, and Function 0 within Device 2 is enable, then the Integrated Graphics registers can be accessed using the IOBAR.

MMIO_Index: MMIO_INDEX is a 32-bit register. An I/O write to this port loads the address of the MMIO register that needs to be accessed. I/O Reads return the current value of this register.

MMIO_Data: MMIO_Data is a 32-bit register. An I/O write to this port is redirected to the MMIO register pointed to by the MMIO-Index register. An I/O read to this port to this is redirected to the MMIO register pointed to by the MMIO-Index register.

10.4 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The MCH supports: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. MCH provides three SMRAM options:

- Below 1MB option that supports compatible SMI handlers.
- Above 1MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1MB, 2MB, or 8MB in size.

The above 1MB solutions require changes to compatible SMRAM handlers code to properly execute above 1MB.

Note: DMI Interface and PCI Express masters are not allowed to access the SMM space.

10.4.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM spaces are not remapped, and therefore the addressed and DRAM SMM spaces are the same address range. Since the High SMM space is remapped, the addressed and DRAM SMM spaces are different address ranges.

Note: The High DRAM spaces are the same as the Compatible Transaction Address space. The table below describes three unique address ranges:

- Compatible Transaction Address (Addr C)
- High Transaction Address (Addr H)
- TSEG Transaction Address (Addr T)

These abbreviations are used later in the table describing SMM Space Transaction Handling.

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (T)	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN

10.4.2 SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang:

1. The Compatible SMM space **must not** be set-up as cacheable.
2. High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any “PCI” devices (including DMI Interface, PCI Express, and graphics devices). This is a BIOS responsibility.
3. Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
4. When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
5. Any address translated through the GMADR TLB must not target DRAM from A_0000-F_FFFF.

10.4.3 SMM Space Combinations

When High SMM is enabled (G_SMRAME=1 and H_SMRAM_EN=1), the Compatible SMM space is effectively disabled. processor originated accesses to the Compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP), otherwise they are forwarded to the DMI Interface. PCI Express and DMI Interface originated accesses are **never** allowed to access SMM space.

Table 10-5. SMM Space Table

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
111	1	1	Disable	Enable	Enable

10.4.4 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at power-up. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM data accesses to be forwarded to the DMI Interface or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

Table 10-6. SMM Control Table

G_SMRAME	D_LCK	D_CLS	D_OPEN	Processor in SMM Mode	SMM Code Access	SMM Data Access
0	X	X	X	X	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	x	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	X	Invalid	Invalid
1	1	1	X	0	Disable	Disable
1	1	0	X	1	Enable	Enable
1	1	1	X	1	Enable	Disable

10.4.5 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI Interface originated transactions are not allowed to SMM space.

10.4.6 Processor WB Transaction to an Enabled SMM Address Space

processor write-back transactions (REQa[1]# = 0) to enabled SMM Address Space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

10.4.7 SMM Access through GTT TLB

Accesses through GTT TLB address translation to enable SMM DRAM space are not allowed. Writes will be routed to memory address 0h with byte enables deasserted and reads will be routed to memory address 0h. If a GTT TLB translated address hits enable SMM DRAM space, the Invalid Translation Entry Flag (ITTEF) in the ERRSTS register is set.

PCI Express and DMI originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enable SMM DRAM space, the Invalid Translation Table Entry Flag (ITTEF) in the ERRSTS register is set.

PCI Express and DMI writes accesses through GMADR range will be snooped. If, when translated, the resulting physical address is to enabled SMM DRAM space, the request will be remapped to address 0h with deasserted byte enables.

PCI Express and DMI read accesses to the GMADR range are not supported, therefore users/systems will be remapped to address 0h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure not in SMM (actually, anything above base of TSEG or 640K-1M). Thus they will be invalid and go to address 0, but that is not specific to PCI Express or DMI; it applies to CPU or internal graphics engines. Also, since the GMADR snoop would not be invalid (because it uses the same translation) and go to address 0.

10.4.8 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into MCH DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as a read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. processor bus transactions are routed accordingly.

10.4.9 I/O Address Space

The MCH does not support the existence of any other I/O devices beside itself on the processor bus. The MCH generates either DMI Interface or PCI Express bus cycles for all processor I/O accesses that it does not claim. Within the host bridge, the MCH contains two internal registers in the processor I/O space, Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA). These locations are used to implement the configuration space access mechanism.

The processor allows 64K+3 bytes to be addressed within the I/O space. The MCH propagates the processor I/O address without any translation on to the destination bus and therefore provides addressability for 64K+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when processor bus HA[16]# address signal is asserted. HA[16]# is asserted on the processor bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HA[16]# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI Interface bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to ICH6 or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to the PCI Express.

The MCH responds to I/O cycles initiated on PCI Express or DMI with a UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 0h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with a UR completion status.

For Pentium® 4 processors, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as 1 transaction. The MCH will break this into 2 separate transactions. This has not been done on previous chipsets. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into 2 transactions by the processor.

10.4.10 PCI Express I/O Address Mapping

The MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in MCH Device 1 configuration space.

10.4.11 MCH Decode Rules and Cross-Bridge Address Mapping

VGAA = 000A_0000 – 000A_FFFF

MDA = 000B_0000 – 000B_7FFF

VGAB = 000B_8000 – 000B_FFFF

MAINMEM = 0100_0000 to TOLUD

10.4.12 Legacy VGA and I/O Range Decode Rules

The legacy 128KB VGA memory range 000A_0000h-000B_FFFFh can be mapped to Internal Graphics (Device 2), to PCI Express (Device 1), and/or to the DMI depending on the programming of the VGA streaming bits. Priority for VGA mapping is constant in that the MCH always decodes internally mapped devices first. Internal to the MCH, decode precedence is always given to the integrated graphics device. The MCH always positively decodes internally mapped devices, namely the integrated graphics and PCI Express. Subsequent decoding bits (VGA Enable & MDAP).

§

11 Functional Description

This chapter describes the MCH interfaces and major functional units.

11.1 Host Interface

The MCH supports the Intel Pentium 4 processor subset of the Enhanced Mode Scalable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped, and a new address can be generated every other bus clock. At 133 MHz or 200 MHz bus clock, the address signals run at 266 MT/s or 400 MT/s for a maximum address queue rate of 66M or 100M addresses/sec, respectively. The data is quad pumped and an entire 64B cache line can be transferred in two bus clocks. At 133 MHz or 200 MHz bus clock, the data signals run at 533 MT/s or 800 MT/s for a maximum bandwidth of 4.3 GB/s or 6.4 GB/s, respectively.

The FSB interface supports up to 12 simultaneous outstanding transactions. The MCH supports only one outstanding Deferred transaction on the FSB.

11.1.1 FSB GTL+ Termination

The MCH integrates GTL+ termination resistors on die. Also, approximately 2.8 pf (fast) – 3.3 pf (slow) per pad of on-die capacitance is implemented to provide better FSB electrical performance.

11.1.2 FSB Dynamic Bus Inversion

The MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the MCH. HDINV[3:0]# indicate if the corresponding 16-bits of data are inverted on the bus for each quad pumped data phase:

HDINV[3:0]#	Data Bits
HDINV0#	HD[15:0]#
HDINV1#	HD[31:16]#
HDINV2#	HD[47:32]#
HDINV3#	HD[63:48]#

Whenever the processor or the MCH drives data, each 16 bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding HDINV# signal is asserted, and the data inverted prior to being driven on the bus. Whenever the processor or the MCH receives data, it monitors HDINV[3:0]# to determine if the corresponding data segment should be inverted.

11.1.3 APIC Cluster Mode Support

This is required for backwards compatibility with existing software, including various OSes. As one example, beginning with Microsoft Windows 2000 there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

- The MCH supports three types of interrupt redirection:
- Physical
- Flat-Logical
- Clustered-Logical

11.2 System Memory Controller

This section describes the MCH system memory interface for DDR/DDR2 memory. The MCH supports DDR/DDR2 memory and either one or two DIMMs per channel.

11.2.1 Memory Organization Modes

The system memory controller supports two styles of memory organization (Interleaved and Asymmetric) and two modes of operation (DDR and DDR2). Rules for populating DIMM slots are included in this chapter.

Table 11-1. Sample System Memory Organization with Interleaved Channels

Rank	Channel A Population	Cumulative Top Address in Channel A	Channel B Population	Cumulative Top Address in Channel B
3	0 MB	2560 MB	0 MB	2560 MB
2	512 MB	2560 MB	256 MB	2560 MB
1	512 MB	1792 MB	512 MB	1792 MB
0	256 MB	768 MB	512 MB	768 MB

Table 11-2. Sample System Memory Organization with Asymmetric Channels

Rank	Channel A Population	Cumulative Top Address in Channel A	Channel B Population	Cumulative Top Address in Channel B
3	0 MB	1280 MB	0 MB	2560 MB
2	256 MB	1280 MB	256 MB	2560 MB
1	512 MB	1024 MB	512 MB	2304 MB
0	512 MB	512 MB	512 MB	1792 MB

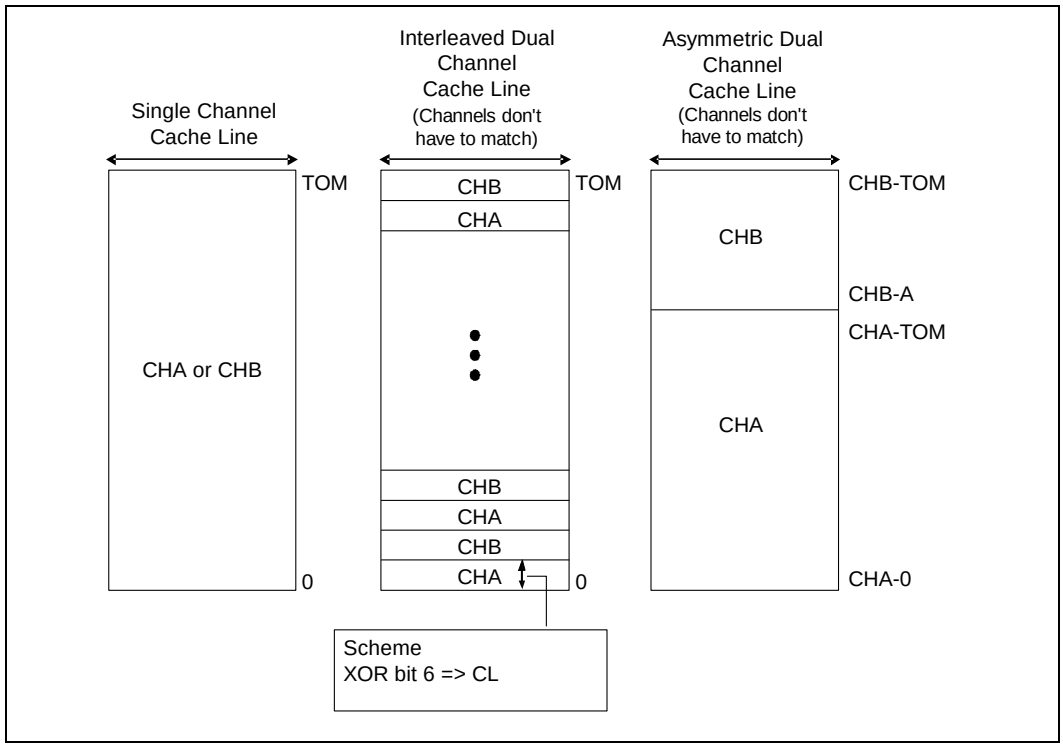
11.2.2 Interleaved Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels, and the switch happens after each cache line (64 byte boundary). If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels. The drawbacks of Interleave Mode is that the system designer must populate both channels of memory such that they have equal capacity, but the technology and device width may vary from one channel to the other.

11.2.3 Asymmetric Mode

Asymmetric mode trades performance for system design flexibility. Unlike the previous mode, addresses start in channel A and stay there until the end of the highest rank in channel A. Then addresses continue from the bottom of channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel. The system designer is free to populate or not to populate any rank on either channel, including either degenerate single channel case.

Figure 11-1. System Memory Styles



11.3 System Memory Configuration Registers Overview

The configuration registers located in the PCI configuration space of the MCH control the System Memory operation. Following is a brief description of configuration registers used the MCH for proper operation of the memory subsystem.

DRAM Rank Boundary (CxDRBy): The “x” represents a channel, either A or B. The “y” represents a rank, 0 through 3. DRB registers define the upper addresses for a rank of DRAM devices in a channel. When the MCH is configured in asymmetric mode, each register represents a single rank. When the MCH is configured in a dual interleaved mode, each register represents a pair of corresponding ranks in opposing channels. There are 4 DRB registers for each channel.

DRAM Rank Architecture (CxDRAy): The “x” represents a channel, either A or B. The “y” represents a rank, 0 through 3. DRA registers specify the architecture features of each rank of devices in a channel. The only architecture feature specified is page size. When MCH is configured in asymmetric mode, each DRA represents a single rank in a single channel. When MCH is configured in a dual-channel interleaved mode, each DRA represents a pair of corresponding ranks in opposing channels. There are 4 DRA registers per channel. Each requires only 3 bits, so there are two DRAs packed into a byte.

Clock Configuration (CLKCFG): Specifies DRAM frequency. The same clock frequency will be driven to all DIMMs.

DRAM Timing (CxDRTy): The “x” represents a channel, A or B. This register grew too large for a single 32-bit access, so a second register was added, differentiated by “y”, A or B. The DRT registers define the timing parameters for all devices in a channel. The BIOS programs this register with “least common denominator” values after reading the SPD registers of each DIMM in the channel.

DRAM Control (CxDRCy): The “x” represents a channel, A or B. This register grew too large for a single 32-bit access, so a second register was added, differentiated by “y”, 0 or 1. DRAM refresh mode, rate, and other controls are selected here.

11.3.1 DRAM Technologies and Organization

All standard 256 Mb, 512 Mb, and 1 Gb technologies and addressing are supported for both x8 and x16 devices.

- All supported DDR2 devices have 4 or 8 banks.
- The MCH supports various page sizes. Page size is individually selected for every rank.
- 4 KB, 8 KB, and 16K B for asymmetric, interleaved, or single channel modes.
- The DRAM sub-system supports single or dual channels, 64b (72b with ECC) wide per channel.
- There can be a maximum of 4 ranks populated (2 Double Sided DIMMs) per channel.
- Mixed mode Double sided DIMMs are not supported.
- By using 1Gb technology, the largest memory capacity is 8 GB (32M rows/bank • 4 banks/device • 8 columns • 8 devices/rank • 4 ranks/channel • 2 channel • 1b/(row • column) • 1G/1024M • 1B/8b = 8 GB). Though it is possible to put 8 GB in system by stuffing both channels this way, the MCH is still limited to 4 GB of addressable space due to the number of address pins on the FSB.

- By using 256 Mb technology, the smallest memory capacity is 128 MB (4M rows/bank • 4 banks/device • 16 columns • 4 devices/rank • 1 rank • 1B/8b = 128 MB)

11.3.1.1 Rules for Populating DIMM Slots

- In all modes, the frequency of System Memory will be the lowest frequency of all DIMMs in the system, as determined through the SPD registers on the DIMMs.
- In the Single Channel mode, any DIMM slot within the channel may be populated in any order. Either channel may be used. To save power, do not populate the unused channel.
- In Dual Channel Asymmetric mode, any DIMM slot may be populated in any order.
- In Dual Channel Interleaved mode, any DIMM slot may be populated in any order, but the total memory in each channel must be the same.

11.3.1.2 System Memory Supported Configurations

The Intel E7221 MCH supports the 256Mbit, 512Mbit and 1Gbit technology based DIMMs from Table 11-3

Table 11-3. DDR/DDR2 DIMM Supported Configurations

Technology	Configuration	# of Row Address Bits	# of Column Address Bits	# of Bank Address Bits	Page Size	Rank Size
256Mbit	16M X 16	13	9	2	4K	128MK
256Mbit	32M X 8	13	10	2	8K	256MB
512Mbit	32M X 16	13	10	2	8K	256MB
512Mbit	64M X 8	13	11	2	16K	512MB
512Mbit	64M X 8	14	10	2	8K	512MB
1Gbit	64M X 16	14	10	2	8K	512MB
1Gbit	128M X 8	14	11	2	16K	1GB
1Gbit	64M X 16	13	10	3	8K	512MB
1Gbit	128M X 8	14	10	3	8K	1GB

11.3.1.3 Main Memory DRAM Address Translation and Decoding

The following tables specify the host interface to memory interface address multiplex for the Intel E7221 MCH. Please refer to the details of the various DIMM configurations as described in Table 11-3 of this document. The address lines specified in the column header refer to the host (CPU) address lines.

Table 11-4. DRAM Address Translation (Single/Dual Channel Asymmetric Mode)

Tech	Banks	Page Size	Rank Size	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
256 Mb x16	4i	4 KB	128 MB						r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	r 12	b 0	b 1	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0
256 Mb x8	4i	8 KB	256 MB					r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0
512 Mb x16	4i	8 KB	256 MB					r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0
512 Mb x8	4i	16 KB	512 MB				r 11	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	b 0	b 1	c 11	c 9	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0
512 Mb x16	4i	8 KB	256 MB					r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0
512 Mb x8	4i	8 KB	512 MB				r 13	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0
1 Gb x16	4i	8 KB	512 MB				r 13	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0
1 Gb x8	4i	16 KB	1 GB			r 13	r 11	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	b 0	b 1	c 11	c 9	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0
1 Gb x16	8i	8 KB	512 MB				r 11	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	b 0	b 1	b 2	c 9	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0
1 Gb x8	8i	8 KB	1 GB			r 13	r 11	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	b 0	b 1	b 2	c 9	c 8	c 7	c 6	c 5	c 4	c 3	c 2	c 1	c 0

Note: b - 'bank' select bit
c - 'column' address bit
r - 'row' address bit

Table 11-5. DRAM Address Translation (Dual Channel Symmetric Mode) (Sheet 1 of 2)

Tech	Banks	Page Size	Rank Size	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
256 Mb x16	4i	4 KB	128 MB						r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	r 12	b 0	b 1	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0
256 Mb x8	4i	8 KB	256 MB					r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0
512 Mb x16	4i	8 KB	256 MB					r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0
512 Mb x8	4i	16 KB	512 MB				r 11	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	b 0	b 1	c 11	c 9	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0
512 Mb x16	4i	8 KB	256 MB					r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0
512 Mb x8	4i	8 KB	512 MB				r 13	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0
1 Gb x16	4i	8 KB	512 MB				r 13	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	r 11	b 1	b 0	c 9	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0

Table 11-5. DRAM Address Translation (Dual Channel Symmetric Mode) (Sheet 2 of 2)

Tech	Banks	Page Size	Rank Size	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
1 Gb x8	4i	16 KB	1 GB			r 13	r 11	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	b 0	b 1	c 11	c 9	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0
1 Gb x16	8i	4 KB	512 MB				r 11	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	b 0	b 1	b 2	c 9	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0
1 Gb x8	8i	8 KB	1 GB			r 13	r 11	r 12	r 10	r 9	r 8	r 7	r 6	r 5	r 4	r 3	r 2	r 1	r 0	b 0	b 1	b 2	c 9	c 8	c 7	c 6	c 5	c 4	h	c 2	c 1	c 0

Note: b - ‘bank’ select bit
c - ‘column’ address bit
h - ‘channel’ select bit
r - ‘row’ address bit

11.3.2 Memory Detection and Initialization

The BIOS detects DRAM devices installed in the platform by querying the SPD registers on the DIMMs, via the ICH6 SMBus. The BIOS initializes the DRAM devices by programming the MCH’s CxDRBy, CxDRAy, CxDRTy, and CxDRCy registers appropriately. The following steps need to be executed to initialize the memory. Ensure that the CPU cache is disabled prior to executing these steps:

1. Verify that all DIMMs present are DDR or DDR2.
2. Verify that all DIMMs present are Unbuffered.
3. Verify that all DIMMs are single- or double-sided. Mixed DIMMs are not supported. (Note: Mixed DIMMs are different memory sizes per rank (side) of a double sided DIMM. If an DIMM is double sided it has to have the same memory size per rank (side)
4. Verify that all DIMMs are either x8 or x16 width.
5. Determine common CAS latencies between all DIMMs and Intel E7221 MCH.
6. Choose common frequency and CAS latency that can be supported.
   - For each product-supported frequency, starting with highest:
   - Starting with smallest CAS latency as determine in step #6:
   - For each DIMM, verify tCLK and tAC parameters reported by the SPD at the frequency and performed grade under consideration against the values required by the JEDEC specification.
   - If the SPD value indicate that either tCLK or tAC does not meet the required timing parameters, then select next large CAS latency and try again.
   - If all CAS latencies fail to meet the required timing parameters for tCLK and tAC, select next lower frequency, and try again.
   - If all frequencies fail to meet the required timing parameters for tCLK and tAC, then the DIMM cannot be supported. This is an error condition, and appropriate action could include posting an error code to the debug port and halting the system.
7. Determine the smallest common tRAS for all DIMMs.

8. Determine the smallest common tRP for all DIMMs.
9. Determine the smallest common tRCD for all DIMMs.
10. Determine the smallest refresh period required by all DIMM.
11. Verify that a burst length of 8 is supported by the DIMMs.
12. Determine the DIMM configuration. This is done via a lookup table and is implementation-specific. This number will be used as a row-index for accessing various tables for programming RCVEN and buffer strength multipliers.
13. Verify that the Intel® E7221 MCH frequency bits are set to operate at the correct Front Side Bus, System Memory Frequency.
14. Determine the mode of operation for the memory channel and program the MCH registers for the memory channel operation.
15. Program Receive Enable Reference Output Timing Control Registers. The values are dependent on the selected frequency of operation, the selected CAS latency, and DIMM configuration.
16. Program the DQS DLL Timing Control Registers. The values are dependent on the selected frequency of operation.
17. Programed the RCOMP SRAM registers. The value are dependent on DIMM configuration (determine in Step #12).
18. Program the DRAM Clock Crossing Registers.
19. Program the DRAM Timing & DRAM Control Registers.
20. Program the DRAM Row Attribute and DRAM Row Boundary registers. The value depend on the DIMM technology and row population.
21. Performed JEDEC initialization for all memory rows.

Note: System BIOS should ensure that the FCSEN bit is clear (C0/1DRC0, Device 0, MCHBAR Space Offset 120h/1A0h, bit 17 = 0) prior to JEDEC commands being executed.

22. Disable all the clocks on the unpopulated rows.
23. Program the DRAM Throttling Register and the DIMM Throttling Event Registers.
24. Prepare MCH for normal operation. Program the DRAM channel Control register (MCH, MCHBAR space Offset 120h/1A0h, bit 17 = 1) prior to JEDEC commands being executed.
    - — Program the refresh period (bits 10:8) with the value determine in step #11.
    - — Program the Mode Select (bits 18:16 of DCC) to ‘111b’ (normal mode).
    - — Program Initialization Complete (bit 19 of DCC to ‘1b’.
25. **System BIOS does a config write to clear (set to “0”) the DRAM Initialization bit located at Device, Function 0, Offset A2h, bit 7 to allow warm reset handling without a power cycle.**

Note: For complete initialization algorithms and their implementation, refer to appropriate BIOS documents through your field representative.

11.3.3 DRAM Clock Generation

The MCH generates three differential clock pairs for every supported DIMM. There are a total of six clock pairs directly driven by the MCH to two DIMMs per channel.

11.3.4 DDR2 On-Die Termination

On die termination (ODT) is a feature that allows a DRAM to turn on/off internal termination resistance for each DQ, DM, DQS, and DQS# signal for x8 and x16 configurations via the ODT control signals. The ODT feature is designed to improve signal integrity of the memory channel by allowing the termination resistance for the DQ, DM, DQS, and DQS# signals to be located inside the DRAM devices themselves instead of on the motherboard. The MCH drives out the required ODT signals, based on memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted DIMM rank to enable or disable their termination resistance.

Note: On-Die terminations is not integrated onto DDR DRAM devices. Therefore system designers must properly terminate on the motherboard, when supporting DDR memory.

11.3.5 DDR2 Off-Chip Driver (OCD) Impedance Calibration

The OCD impedance adjustment mode allows the MCH to measure and adjust the pull-up and pull-down strength of the DRAM devices. It uses a series of EMRS commands to guide the DRAM through measurement and calibration cycles. This feature is described in more detail in the JEDEC DDR2 device specification.

The algorithm and sequence of the adjustment cycles is handled by software. The MCH adjusts the DRAM driver impedance by issuing OCD commands to the DIMM and looking at the analog voltage on the DQ lines.

11.4 PCI Express

Refer to Chapter 1 for a list of PCI Express features, the *PCI Express Specification* for further details.

This MCH is part of a PCI Express root complex. This means it connects a host processor/memory subsystem to a PCI Express hierarchy.

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 2.5 GHz (250 MHz internally) results in 2.5 Gb/s/direction which provides a 250 MB/s communications channel in each direction (500 MB/s total) that is close to twice the data rate of classic PCI per lane.

11.4.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

Note: If the MCH receives two back-to-back malformed packets, the second malformed packet is not trapped or logged. The MCH will not log or identify the second malformed packet. However, the 1st malformed TLP is logged, and is considered a Fatal Error. Link behavior is not guaranteed at that point whether a 2nd malformed TLP is detected or not.

11.4.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

11.4.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

11.5 Power Management

Power Management capabilities of the MCH include the following:

- ACPI 1.0b support
- ACPI S0, S4, S5, C0, C1, C2, C3, C4
- Enhanced power management state transitions for increasing time processor spends in low power states
- Graphics Adapter States: D0, D3
- PCI Express Link States: L0, L0s, L1, L2/L3 Ready, L3
- PM_THRMTRIP# output
- Conditional memory Self-Refresh during C2, C3, and C4 states

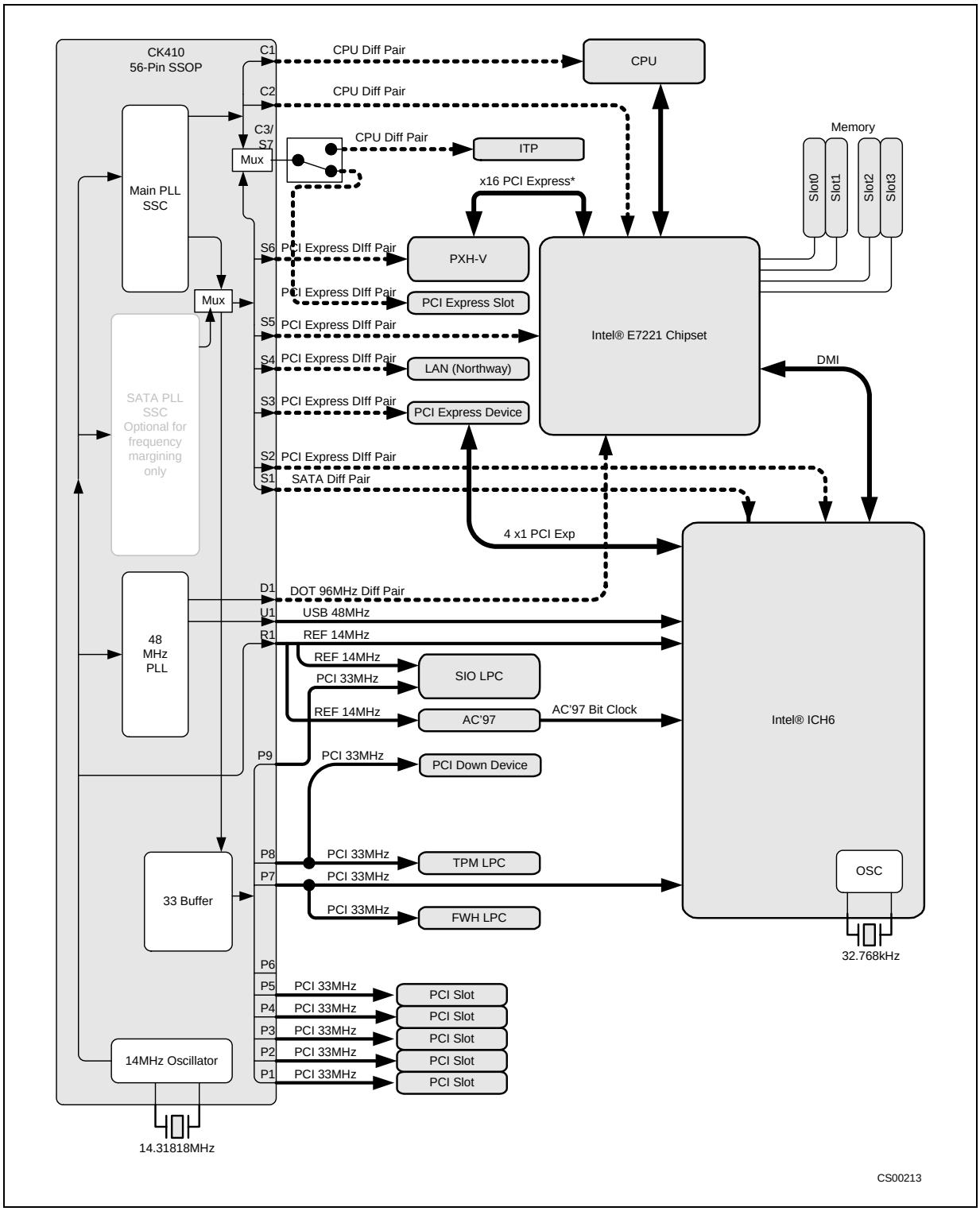
11.6 Clocking

The MCH has PLLs to provide the internal clocks.

- Host PLL - This PLL generates the main core clocks in the host clock domain. The host PLL is used to generate memory and internal graphics core clocks. It uses the Host clock (HCLKIN) as a reference.
- PCI Express PLL - This PLL generates all PCI Express related clocks, including the Direct Media Interface that connects to the ICH6. This PLL uses the 100 MHz (GCLKIN) as a reference.

Figure 11-2 illustrates the various clocks in the platform.

Figure 11-2. System Clocking Diagram



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12 Electrical Characteristics

This chapter contains the MCH absolute maximum electrical ratings, power dissipation values, and DC characteristics.

12.1 Absolute Maximum Ratings

Table 12-1 lists the Intel E7221 MCH's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the AC and DC tables.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "operating conditions" is not recommended and extended exposure beyond "operating conditions" may affect reliability.

Table 12-1. Absolute Maximum Ratings (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	Notes
$T_{storage}$	Storage Temperature	-55	150	°C	1
MCH Core					
VCC	1.5V Core Supply Voltage with respect to VSS	-0.3	1.65	V	
Host Interface (533 MHz/800 MHz)					
VTT	1.2V System Bus Input Voltage with respect to VSS	-0.3	1.65	V	
VCCA_HPLL	1.5V Host PLL Analog Supply Voltage with respect to VSS	-0.3	1.65	V	
DDR Interface (333 MHz/400 MHz)					
VCCSM (DDR)	2.6V DDR System Memory Supply Voltage with respect to VSS	-0.3	4.0	V	
VCCA_SMPLL (DDR)	1.5V System Memory PLL Analog Supply Voltage with respect to VSS	-0.3	1.65	V	
DDR2 Interface (400 MHz/533 MHz)					
VCCSM (DDR2)	1.8V DDR2 System Memory Supply Voltage with Respect to VSS	-0.3	4.0	V	
VCCA_SMPLL (DDR2)	1.5V System Memory PLL Analog Supply Voltage with respect to VSS	-0.3	1.65	V	
PCI Express/DMI Interface					
VCC_EXP	1.5V PCI Express* and DMI Supply Voltage with respect to VSS	-0.3	1.65	V	
VCCA_EXPPLL	1.5V PCI Express PLL Analog Supply Voltage with respect to VSS	-0.3	1.65	V	

Table 12-1. Absolute Maximum Ratings (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Notes
RGB/CRT DAC Display Interface (8 bit)					
VCCA_DAC	2.5V Display DAC Analog Supply Voltage with respect to VSS	-0.3	2.65	V	
VCCA_DPLLA	1.5V Display PLL A Analog Supply Voltage with respect to VSS	-0.3	1.65	V	
VCCA_DPLLB	1.5V Display PLL B Analog Supply Voltage with respect to VSS	-0.3	1.65	V	
CMOS Interface					
VCC2	2.5V CMOS Supply Voltage with respect to VSS	-0.3	2.65	V	

NOTE: Possible damage to the MCH may occur if the MCH temperature exceeds 150°C. Intel does not guarantee functionality for parts that have exceeded temperatures above 150°C due to spec violation.

12.2 Power Characteristics

Table 12-2. Non Memory Power Characteristics

Symbol	Parameter	Signal Names	Min	Typ	Max	Unit	Notes
I_{VTT}	1.2V System Bus Supply Bus Current	VTT	—	—	1.0	A	1, 4
I_{VCC}	1.5V Core Supply Current (Integrated)	VCC	—	—	9.7	A	2,3,4
I_{VCC}	1.5V Core Supply Current (Discrete)	VCC	—	—	7.7	A	2,3,4
I_{VCC_EXP}	1.5V PCI Express* and DMI Supply Current	VCC_EXP	—	—	1.4	A	
I_{VCCA_DAC}	2.5V Display DAC Analog Supply Current	VCCA_DAC	—	—	70	mA	
I_{VCC2}	2.5V CMOS Supply Current	VCC2	—	—	2	mA	
I_{VCCA_EXPPLL}	1.5V PCI Express and DMI PLL Analog Supply Current	VCCA_EXPPLL	—	—	45	mA	
I_{VCCA_HPLL}	1.5V Host PLL Supply Current	VCCA_HPLL	—	—	45	mA	
I_{VCCA_DPLLA} I_{VCCA_DPLLB}	1.5V Display PLL A and PLL B Supply Current	VCCA_DPLLA VCCA_DPLLB	—	—	55	mA	

NOTES:
1. Estimate is only for max current coming through Chipset's supply balls
2. Rail includes PLL current
3. Includes Worst case Leakage
4. Calculated for highest frequencies

Table 12-3. DDR (333MHz/400MHz) Power Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
I_{VCCSM} (DDR)	DDR System Memory Interface (2.6 V) Supply Current	—	4.1	A	
I_{SUS_VCCSM} (DDR)	DDR System Memory Interface (2.6 V) ***Standby*** Supply Current	—	TBD	mA	
I_{SMVREF} (DDR)	DDR System Memory Interface Reference Voltage (1.3 V) Supply Current	—	10	µA	
I_{SUS_SMVREF}	DDR System Memory Interface Reference Voltage (1.3 V) ***Standby*** Supply Current	—	10	µA	
I_{TTRC} (DDR)	DDR System Memory Interface Resistor Compensation Voltage (2.6 V) Supply Current	—	42	mA	
I_{SUS_TTRC} (DDR)	DDR System Memory Interface Resistor Compensation Voltage (2.6 V) ***Standby*** Supply Current	—	0	µA	
I_{VCCA_SMPLL} (DDR)	System Memory PLL Analog (1.5 V) Supply Current	—	60	mA	

Table 12-4. DDR2 (400MHz/533MHz) Power Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
I_{VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V) Supply Current	—	4.7	A	
I_{SUS_VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V) ***Standby*** Supply Current	—	25	mA	
I_{SMVREF} (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) Supply Current	—	10	µA	
I_{SUS_SMVREF} (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) ***Standby*** Supply Current	—	10	µA	
I_{TTRC} (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Supply Current	—	32	mA	
I_{SUS_TTRC} (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) ***Standby*** Supply Current	—	0	µA	
I_{VCCA_SMPLL} (DDR2)	System Memory PLL Analog (1.5 V) Supply Current	—	60	mA	

12.3 Signal Groups

The signal description includes the type of buffer used for the particular signal:

GTL+ Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details. The Intel® E7221 chipset MCH integrates most GTL+ termination resistors.

DDR DDR System memory (2.6 V CMOS buffers)

DDR2 DDR2 System memory (1.8 V CMOS buffers)

PCI Express PCI Express interface signals. These signals are compatible with PCI Express 1.0a signaling environment AC Specifications. The buffers are ***not*** 3.3 V tolerant.

Analog Analog signal interface

Ref Voltage reference signal

HVCMOS 2.5 V Tolerant High Voltage CMOS buffers

SSTL-2 2.6 V Tolerant Stub Series Termination Logic

SSTL-1.8 1.8 V Tolerant Stub Series Termination Logic

Table 12-5. Signal Groups (Sheet 1 of 3)

Signal Group	Signal Type	Signals	Notes
Host Interface Signal Groups			
(a)	GTL+ Input/Outputs	HADS#, HBNR#, HBREQ0#, HDBSY#, HDRDY#, HDINV[3:0]#, HA[31:3]#, HADSTB[1:0]#, HD[63:0], HDSTBP[3:0]#, HDSTBN[3:0]#, HHIT#, HHITM#, HREQ[4:0]#, HLOCK#	
(b)	GTL+ Common Clock Outputs	HBPRI#, HCPURST#, HDEFER#, HTRDY#, HRS[2:0]#, HDPWR#, HEDRDY#	
(c)	GTL+ Asynchronous Input	BSEL[2:0], HPCREQ#	
(d)	Analog Host I/F Ref & Comp. Signals	HVREF, HSWING, HRCOMP, HSCOMP	
PCI Express* Interface Signal Groups			
(e)	PCI Express Input	**PCI Express Interface:** EXP_RXN(7:0), EXP_RXP(7:0),	
(f)	PCI Express Output	**PCI Express Interface:** EXP_TXN(7:0), EXP_TXP(7:0)	
(g)	Analog PCI Express I/F Compensation Signals	EXP_COMP0, EXP_COMPI	

Table 12-5. Signal Groups (Sheet 2 of 3)

Signal Group	Signal Type	Signals	Notes
DDR Interface Signal Groups			
(h)	SSTL-2 DDR CMOS I/O	SDQ_A[63:0], SDQ_B[63:0] SDQS_A[7:0], SDQS_B[7:0]	
(i)	SSTL-2 DDR CMOS Output	SDM_A[7:0], SDM_B[7:0], SMA_A[13:0], SMA_B[13:0], SBS_A[1:0], SBS_B[1:0], SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B#, SCKE_A[3:0], SCKE_B[3:0], SCS_A[3:0]#, SCS_B[3:0]#, SCLK_A[5:0], SCLK_A[5:0]#, SCLK_B[5:0], SCLK_B[5:0]#	
(j)	DDR Reference Voltage	SMVREF[1:0] (DDR)	
DDR2 Interface Signal Groups			
(k)	SSTL – 1.8 DDR2 CMOS I/O	SDQ_A[63:0]#, SDQ_B[63:0]#, SDQS_A[7:0], SDQS_A[7:0]#, SDQS_B[7:0], SDQS_B[7:0]#)	
(l)	SSTL – 1.8 DDR2 CMOS Output	SDM_A[7:0], SDM_B[7:0], SMA[13:0], SMA_B[13:0], SBS_A[2:0], SBS_B[2:0], SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B#, SODT_A[3:0], SODT_B[3:0], SCKE_A[3:0], SCKE_B[3:0], SCS_A[3:0]#, SCS_B[3:0]#, SCLK_A[5:0], SCLK_A[5:0]#, SCLK_B[5:0], SCLK_B[5:0]#	
(m)	DDR2 Reference Voltage	SMVREF[1:0] (DDR2)	
RGB/CRT DAC Display Signal Groups			
	Analog Current Outputs	RED, RED#, GREEN, GREEN#, BLUE, BLUE#	
	Analog/Ref DAC Miscellaneous	REFSET	Current Mode Reference pin. DC Spec. not required
	CMOS Type	HSYNC, VSYNC	
Clocks, Reset, and Miscellaneous Signal Groups			
(n)	HVCMOS Input	EXTTS#	
(n1)	Miscellaneous Inputs	RSTIN#, PWROK	
(0)	Low Voltage Diff. Clock Input	HCLKN, HCLKP, DREFCLKP, DREFCLKN, GCLKP, GCLKN	
(p)	HVCMOS I/O	DDC_CLK, DDC_DATA	

Table 12-5. Signal Groups (Sheet 3 of 3)

Signal Group	Signal Type	Signals	Notes
I/O Buffer Supply Voltages			
(q)	1.2V System Bus Input Supply Voltage	VTT	
(r)	1.5V PCI Express Supply Voltages	VCC_EXP	
(s)	2.6V DDR Supply Voltage	VCCSM (DDR)	
(t)	1.8V DDR2 Supply Voltage	VCCSM (DDR2)	
(u)	1.5V DDR PLL Analog Supply Voltage	VCCA_SMPLL (DDR)	
(v)	1.5V DDR2 PLL Analog Supply Voltage	VCCA_SMPLL (DDR2)	
(w)	1.5V MCH Core Supply Voltage	VCC	
(x)	2.5V CMOS Supply Voltage	VCC2	
(y)	2.5V RGB/CRT DAC Display Analog Supply Voltage	VCCA_DAC	
(z)	PLL Analog Supply Voltages	VCCA_HPLL, VCCA_EXPPLL, VCCA_DPLLA, VCCA_DPLLB	

12.4 General DC Characteristics

Table 12-6. DC Characteristics[3] (Sheet 1 of 4)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I/O Buffer Supply Voltage (AC Noise not included)							
VCCSM (DDR)	(s)	DDR I/O Supply Voltage	2.5	2.6	2.7	V	
VCCSM (DDR2)	(t)	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	
VCCA_SMPLL (DDR)	(u)	DDR I/O PLL Analog Supply Voltage	1.425	1.5	1.575	V	
VCCA_SMPLL (DDR2)	(v)	DDR2 I/O PLL Analog Supply Voltage	1.425	1.5	1.575	V	
VCC_EXP	(r)	PCI Express Supply Voltage	1.425	1.5	1.575	V	
VTT	(q)	System Bus Input Supply Voltage	1.09	1.2	1.26	V	
VCC	(w)	MCH Core Supply Voltage	1.425	1.5	1.575	V	
VCC2	(x)	CMOS Supply Voltage	2.375	2.5	2.625	V	
VCCA_DAC	(y)	CRT Display DAC Supply Voltage	2.375	2.5	2.625	V	
VCCA_HPLL, VCCA_EXPPLL, VCCA_DPLLA, VCCA_DPLLB	(z)	Various PLL'S Analog Supply Voltages	1.425	1.5	1.575	V	
Reference Voltages							
HVREF	(d)	Host Address, Data, and Common Clock Signal Reference Voltage	2/3 x VTT – 2%	2/3 x VTT	2/3 x VTT + 2%	V	
HSWING	(d)	Host Compensation Reference Voltage	1/4 x VTT – 2%	1/4 x VTT	1/4xVTT + 2%	V	
SMVREF (DDR)	(j)	DDR Reference Voltage	0.50x VCCSM (DDR) – 0.05	0.50x VCCSM (DDR)	0.50x VCCSM (DDR) + 0.05	V	
SMVREF (DDR2)	(m)	DDR2 Reference Voltage	0.49x VCCSM (DDR2)	0.50x VCCSM (DDR2)	0.51x VCCSM (DDR2)	V	

Table 12-6. DC Characteristics[3] (Sheet 2 of 4)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
Host Interface							
V_{IL_H}	(a, c)	Host GTL+ Input Low Voltage	-0.10	0	(2/3 x VTT) – 0.1	V	
V_{IH_H}	(a, c)	Host GTL+ Input High Voltage	(2/3 x VTT) + 0.1	VTT	VTT + 0.1	V	
V_{OL_H}	(a, b)	Host GTL+ Output Low Voltage			(0.25 x VTT) + 0.1	V	
V_{OH_H}	(a, b)	Host GTL+ Output High Voltage	VTT – 0.1		VTT	V	
I_{OL_H}	(a, b)	Host GTL+ Output Low Current			VTT_{max} / (1-0.25) Rtt_{min}	mA	Rtt_{min} = 54 Ω
I_{LEAK_H}	(a, c)	Host GTL+ Input Leakage Current			20	µA	V_{OL}<Vpad< Vtt
C_{PAD}	(a, c)	Host GTL+ Input Capacitance	2		3.5	pF	
C_{PCKG}	(a, c)	Host GTL+ Input Capacitance (common clock)	0.90		2.5	pF	
DDR Interface							
$V_{IL(DC)}$ (DDR)	(h)	DDR Input Low Voltage			SMVREF (DDR) – 0.15	V	
$V_{IH(DC)}$ (DDR)	(h)	DDR Input High Voltage	SMVREF (DDR) + 0.15			V	
$V_{IL(AC)}$ (DDR)	(h)	DDR Input Low Voltage			SMVREF (DDR) – 0.31	V	
$V_{IH(AC)}$ (DDR)	(h)	DDR Input High Voltage	SMVREF (DDR) + 0.31			V	
V_{OL} (DDR)	(h, i)	DDR Output Low Voltage			0.4	V	1
V_{OH} (DDR)	(h, i)	DDR Output High Voltage	2.1			V	1
I_{Leak} (DDR)	(h)	Input Leakage Current			±10	µA	
$C_{I/O}$ (DDR)	(h, i)	DDR Input/Output Pin Capacitance	3.0		6.0	pF	

Table 12-6. DC Characteristics[3] (Sheet 3 of 4)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
DDR2 Interface							
$V_{IL(DC)}$ (DDR2)	(k)	DDR2 Input Low Voltage			SMVREF (DDR2) – 0.125	V	
$V_{IH(DC)}$ (DDR2)	(k)	DDR2 Input High Voltage	SMVREF (DDR2) + 0.125			V	
$V_{IL(AC)}$ (DDR2)	(k)	DDR2 Input Low Voltage			SMVREF (DDR2) – 0.250	V	
$V_{IH(AC)}$ (DDR2)	(k)	DDR2 Input High Voltage	SMVREF (DDR2) + 0.250			V	
V_{OL} (DDR2)	(k, l)	DDR2 Output Low Voltage			0.3	V	1
V_{OH} (DDR2)	(k, l)	DDR2 Output High Voltage	1.5			V	1
I_{Leak} (DDR2)	(k)	Input Leakage Current			±10	µA	
$C_{I/O}$ (DDR2)	(k, l)	DDR2 Input/Output Pin Capacitance	3.0		6.0	pF	
1.5V PCI Express* Interface 1.0a							
$V_{TX-DIFF\ P-P}$	(f)	Differential Peak to Peak Output Voltage	0.400		0.600	V	2
V_{TX_CM-ACp}	(f)	AC Peak Common Mode Output Voltage			20	mV	
$Z_{TX-DIFF-DC}$	(f)	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX-DIFF\ p-p}$	(e)	Differential Peak to Peak Input Voltage	0.175		0.600	V	3
V_{RX_CM-ACp}	(e)	AC peak Common Mode Input Voltage			150	mV	
Clocks, Reset, and Miscellaneous Signals							
V_{IL}	(n)	Input Low Voltage			0.8	V	
V_{IH}	(n)	Input High Voltage	2.0			V	
I_{LEAK}	(n)	Input Leakage Current			±10	µA	
C_{IN}	(n)	Input Capacitance	3.0		6.0	pF	
V_{IL}	(o)	Input Low Voltage		0		V	
V_{IH}	(o)	Input High Voltage	0.660	0.710	0.850	V	
V_{CROSS}	(o)	Crossing Voltage	0.45 x (V_{IH} - V_{IL})	0.5 x (V_{IH} - V_{IL})	0.55 x (V_{IH} - V_{IL})	V	
C_{IN}	(o)	Input Capacitance	TBD		TBD	pF	
V_{OL}	(p)	Output Low Voltage (CMOS Outputs)			0.4	V	
V_{OH}	(p)	Output High Voltage (CMOS Outputs)	2.1			V	
I_{OL}	(p)	Output Low Current (CMOS Outputs)			1	mA	@V_{OL_HI} max

Table 12-6. DC Characteristics[3] (Sheet 4 of 4)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I_{OH}	(p)	Output High Current (CMOS Outputs)	-1			mA	@V_{OH_HI} min
V_{IL}	(p)	Input Low Voltage			1.1	V	
V_{IH}	(p)	Input High Voltage	1.4			V	
I_{LEAK}	(p)	Crossing Voltage			±10	µA	
C_{IN}	(p)	Input Capacitance	3.0		6.0	pF	
V_{IL}	(n1)	Input Low Voltage			0.8	V	
V_{IH}	(n1)	Input High Voltage	2.0			V	
I_{LEAK}	(n1)	Crossing Voltage			±100	µA	0 < Vin < VCC3_3
C_{IN}	(n1)	Input Capacitance	4.690		5.370	pF	

NOTES:
1. Determined with 2x MCH DDR/DDR2 Buffer Strength Settings into a 50Ω to 0.5xVCCSM (DDR/DDR2) test load.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI-E specification and measured over any 250 consecutive TX UIs.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load shown in Receiver compliance eye diagram of PCI-E spec should be used as the RX device when taking measurements.

§

13 Ballout and Package Information

This chapter provides the ballout and package information.

13.1 DDR2 Ballout

Figure 13-1 and Figure 13-2 diagram the MCH ballout for platforms using a DDR2 system memory as viewed from the top side of the package. They are broken into a left side view and a right side view of the package. Following the ballmap diagrams are two signal lists; the first is sorted by name and the second is sorted by ball location.

Note: Balls that are listed as RSV are reserved. Board traces should not be routed to these balls.

Note: Balls that are listed as NC are No Connects.

Figure 13-1. Intel® E7221 MCH DDR2 Ballout – Top View, Left Side

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A		NC	VSS		VSS	EXP_TXN3	EXP_TXP3	EXP_TXN1	EXP_TXP1	VSS	GCLKP	VCCA_DPLLA	VCC2	VCCA_EXPPLL	CRTIREFSET	RSV	VCCA_HPLL	VSS
B	NC	VSS	EXP_RXP4	EXP_RXN4	VSS	VSS	VSS	VSS	VSS	VSS	GCLKN	VSS	VCCA_DPLLB	VSS	RSV	VSS	VCCA_SMPLL	VSS
C	VSS	EXP_TXP5	VSS	VSS	EXP_TXN4	EXP_TXP4	EXP_TXN2	EXP_TXP2	EXP_TXN0	EXP_TXP0	VSS		VSS	RSV	MTYPE	NC	VSS	VSS
D		EXP_TXN5	VSS	VSS	EXP_RXP5	VSS	VSS	VSS	VSS	VSS	VSS	CRTVSYNC	VCCA_DAC	CRTGREEN	VSS	VSS	BSEL2	VSS
E	VSS	VSS	EXP_TXP6	VSS	EXP_RXN5	VSS	EXP_RXN3	VSS	EXP_RXN2	VSS	EXP_RXP0	CRTHSYNC	VCCA_DAC	CRTGREEN#	BSEL1	NC	VSS	VSS
F	EXP_TXP7	VSS	EXP_TXN6	VSS	VSS	VSS	EXP_RXP3	VSS	EXP_RXP2	VSS	EXP_RXN0	NC	VSSA_DAC	CRTRED	RSV	VSS	HD47	VSS
G	EXP_TXN7	VSS	RSV	VSS	EXP_RXN6	EXP_RXP6	VSS	VSS	VSS	VSS	VSS	NC	VSS	CRTRED#	VSS	RSV	VSS	HD45
H	RSV	VSS	RSV	VSS	VSS	VSS	EXP_RXN7	EXP_RXP7	VSS	VSS	EXP_RXN1	NC	VSS	CRTBLUE	NC	BSEL0	NC	HD46
J	RSV	VSS	RSV	VSS	RSV	RSV	VSS	VSS	VSS	VSS	EXP_RXP1	NC	RSV	CRTBLUE#	VSS	VSS	VSS	VSS
K	RSV	VSS	RSV	VSS	VSS	VSS	RSV	RSV	VSS	VSS	VSS	NC	RSV	VSS	RSV	EXTTS#	HD44	HD43
L	RSV	VSS	RSV	VSS	RSV	RSV	VSS	VSS	VSS	VCC	VSS	NC	VSS	CRTDDCDATA	VSS	VSS	VSS	VSS
M	RSV	VSS	RSV	VSS	VSS	VSS	RSV	RSV	VSS	VSS	VSS	DREFCLKN	DREFCLKP	ICH_SYNC#	CRTDDCCLK	RSV	VSS	HD42
N	RSV	VSS	RSV	VSS	RSV	RSV	VSS	VSS	VSS	VSS	VSS	NC	VCC	VCC	VCC	VCC	VSS	VCC
P	RSV	VSS	RSV	VSS	VSS	VSS	RSV	RSV	VSS	RSV	VSS	NC	VCC	VCC	VCC	VSS	VCC	VSS
R	RSV	VSS	DMI_TXP0	VSS	RSV	RSV	VSS	VSS	VSS	RSV	VSS	NC	VCC	VCC	VCC	VCC	VSS	VCC
T	DMI_TXP1	VSS	DMI_TXN0	VSS	VSS	VSS	VSS	DMI_RXN1	DMI_RXP1	VSS	VSS	NC	VCC	VCC	VCC	VCC	VCC	VSS
U	DMI_TXN1	VSS	DMI_TXP2	VSS	DMI_RXP0	DMI_RXN0	VSS	VSS	VSS	DMI_RXN3	VSS	NC	VCC	VCC	VSS	VCC	VSS	VCC
V	VSS	VSS	DMI_TXN2	VSS	DMI_TXP3	VSS	DMI_RXP2	DMI_RXN2	VSS	DMI_RXP3	VSS	NC	VCC	VCC	VCC	VSS	VCC	VSS
W	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	DMI_TXN3	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_COMPI	VSS	NC	VCC	VCC	VSS	VCC	VSS	VCC
Y	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_COMPO	VSS	NC	VCC	VCC	VCC	VCC	VCC	VSS
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	VCC	VCC	VSS	VCC	VSS	VCC
AB	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	NC	VCC	VCC	VCC	VCC	VCC	VCC
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	RSV	RSV	RSV	RSV	RSV	RSV	RSV
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	SDQ_B20	VSS	SDQ_B17	SDQ_B29	VSS	SDQ_A29	SDQ_B24
AE	SDQ_A5	SDQ_A4	SDQ_A0	VSS	RSV	VSS	SVREF0	SVREF1	VSS	SMSLEWOUT1	SDQ_B4	VSS	SDQ_B21	SDQ_B19	SDQ_A28	RSV_TP0	SDQ_A24	NC
AF	VSS	SDM_A0	SDQ_A1	VSS	RSV	VSS	RSTIN#	VSS	SMSLEWIN1	VSS	SDQ_B5	SDQ_B11	SDQ_B16	SDQ_B18	SDQ_B28	SDQ_A25	SDM_A3	VSS
AG	SDQS_A0	RSV	SDQ_A6	SRCOMP0	VSS	NC	PWROK	SRCOMP1	VSS	SDQ_B1	SDQ_B0	VSS	VSS	RSV	VSS	VSS	RSV	VSS
AH	VSS	SDQ_A7	SDQ_A2	SDQ_B12	NC	VSS	SDQ_B7	SDQS_B0	RSV	SDM_B0	VSS	SDM_B2	SDQS_B2	VSS	RSV_TP1	SDQS_A3	SDQ_A27	VSS
AJ	SDQ_A12	SDQ_A3	SDQ_A13	VSS	SDQ_B13	SDQ_B3	SDQ_B2	SDQ_B6	VSS	VSS	SCLK_B1#	SMSLEWIN0	VSS	NC	VSS	VSS	SDQ_A31	SCB_B1
AK	VSS	SDQ_A8	SDQ_A9	VSS	SDM_B1	VSS	SDQ_A17	VSS	SCLK_B4	SDQ_B8	VSS	SMSLEWOUT0	SDQ_B22	VSS	RSV_TP3	SDQ_A30	VSS	SCB_B5
AL	SDM_A1	RSV	SDQS_A1	SDQ_B9	RSV	SDQ_B14	SDQ_A19	SDQ_B10	SCLK_B4#	VSS	SCLK_B1	VCCSM	VSS	SDQ_B23	RSV_TP2	VSS	SDQ_A26	SDQ_B26
AM		SCLK_A1	SCLK_A1#	VSS	SDQS_B1	VSS	SDQ_A22	SDQ_A23	SDQ_A18	VCCSM	VCCSM	NC	VCCSM	VCCSM	NC	VCCSM	VCCSM	NC
AN	VSS	SCLK_A4	SCLK_A4#	SDQ_A10	SDQ_A21	SDQ_B15	RSV	SCKE_B1	SCKE_A1	SCKE_A3	SMA_B12		SMA_B8	SMA_B5	SMA_A9	SMA_A7	SMA_B2	SMA_A8
AP	NC	SDQ_A14	SDQ_A15	SDQ_A11	SDQ_A16	SDM_A2	SDQS_A2	VCCSM	SCKE_B0	SCKE_A2	SMA_B11	VCCSM	SMA_A12	SMA_B7	SMA_A11	VCCSM	SMA_B6	SMA_B1
AR	NC	NC	VSS		SDQ_A20	VSS	VCCSM	SCKE_B3	SCKE_B2	VCCSM	SCKE_A0	SMA_B9	VSS	VCCSM	SMA_B4	SMA_B3	VSS	VCCSM
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

Figure 13-2. Intel® E7221 MCH DDR2 Ballout – Top View, Right Side

	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
A	VTT	VTT	VTT	VTT	HSWING	HVREF	HD48	VSS	HD61	HD57	HD55	VSS	HD53		VSS	NC	NC
B	VTT	VTT	VTT	VTT	HRCOMP	VSS	HD63	HDINV3#	HD54	VSS	HDSTBP3#	HD51	HD52	HD15	HD13	HD11	NC
C	VTT	VTT	VTT	VTT	VSS		HD58	HD59	HD49	HD56	HDSTBN3#	HD17	HD50	HD14	HD9	HD12	VSS
D	VTT	VTT	VTT	VTT	VSS	HSCOMP	VSS	VSS	HD60	VSS	HD18	VSS	VSS	VSS	HD10	HD8	
E	VTT	VTT	VTT	VTT	VSS	HD62	HD25	VSS	HD24	HD16	VSS	HBPRI#	HPCREQ#	HREQ1#	HDSTBP0#	HDINV0#	HDSTBN0#
F	HDSTBN2#	VTT	VTT	VTT	VSS	NC	VSS	HDSTBN1#	HD23	HD22	VSS	VSS	HREQ4#	VSS	HREQ0#	HD6	VSS
G	VSS	VSS	VTT	VTT	VSS	HCPURST#	HD26	VSS	VSS	VSS	HD20	HA6#	HREQ3#	HA7#	HD7	HD5	HD3
H	HD41	HD40	VSS	VTT	HD37	VSS	VSS	HDSTBP1#	VSS	HD19	HA3#	VSS	HREQ2#	VSS	HD1	VSS	HD4
J	HDSTBP2#	VSS	HD35	HD32	VSS	HD33	HD27	HDINV1#	HD21	HA13#	HA5#	VSS	HADSTB0#	HRS2#	HD0	HD2	HDEFER#
K	HDINV2#	VSS	HD39	HD34	HD31	VSS	HD28	VSS	HA14#	VSS	HA4#	HA8#	VSS	VSS	HA15#	HRS0#	VSS
L	NC	VSS	VSS	VSS	HD30	VSS	HD29	HA18#	VSS	HA12#	HA9#	VSS	HA11#	VSS	HLOCK#	HHIT#	HDBSY#
M	HD38	VSS	HD36	HCLKN	HCLKP	VSS	VSS	HA20#	VSS	HA16#	VSS	HA10#	HADS#	HDRDY#		VSS	HBNR#
N	VSS	VCC	VCC	NC	NC	NC	VSS	HA19#	HADSTB1#	VSS	HA23#	VSS	HA21#	VSS	HA26#	HTRDY#	HHITM#
P	VCC	VSS	VCC	VCC	NC	NC	VSS	HA22#	VSS	HA24#	VSS	NC	VSS	VSS	HEDRDY#	HRS1#	VSS
R	VSS	VCC	VSS	VCC	VCC	NC	VSS	VSS	VSS	HA25#	HA17#	SCB_A4	SCB_A5	SDQ_A58	HBREQ0#	SDQ_A59	RSV
T	VCC	VCC	VCC	VSS	VCC	VCC	VSS	HA30#	HA27#	VSS	HA31#	VSS	HA28#	VSS	SDQ_A62	VSS	SDQ_A63
U	VSS	VCC	VSS	VCC	VSS	VCC	VSS	SDQ_B63	VSS	HA29#	VSS	RSV	VSS	VSS	SDM_A7	SDQS_A7	RSV
V	VCC	VSS	VCC	VSS	VCC	VCC	VSS	VSS	VSS	SDQ_B58	SDQ_B59	SDQS_A8	SCB_A1	SCB_A0	SDQ_A57	SDQ_A56	VSS
W	VSS	VCC	VSS	VCC	VSS	VCC	VSS	SDQ_B62	SDQS_B7	VSS	SDQ_B57	VSS	SDM_B7	VSS	SDQ_A61	SDQ_A51	SDQ_A60
Y	VCC	VCC	VCC	VSS	VCC	VCC	VSS	SDQ_B60	VSS	RSV	VSS	SCB_A6	VSS	VSS	SDQ_A50	VSS	SDQ_A55
AA	VSS	VCC	VCC	VCC	VCC	VCC	VSS	VSS	VSS	SDQ_B56	SDQ_B61	SCB_A3	SCB_A2	SDQ_A54	SDM_A6	SDQS_A6	RSV
AB	VCC	VCC	VCC	VCC	VCC	VCC	VSS	SDQ_B51	SDQ_B55	VSS	SCB_A7	VSS	SDQS_B6	VSS	SMA_A13	SCLK_A2	VSS
AC	RSV	RSV	RSV	RSV	NC	NC	VSS	SDQ_B50	VSS	SDQ_B54	VSS	RSV	VSS	VSS	SCLK_A2#	SCLK_A5#	SCLK_A5
AD	VSS	VSS	NC	VSS	SDQ_B37	SDM_B6	VSS	VSS	SDQ_A35	SCLK_B5#	SCLK_B5	NC	SDQ_A48	SMA_B13		VSS	SDQ_A49
AE	SDQ_B25	SDM_B3	VSS	VSS	VSS	VSS	SCLK_B2#	SCLK_B2	SDQ_B49	VSS	SDQ_B53	NC	SDQ_B52	VSS	SDQ_A43	SDQ_A53	SDQ_A52
AF	NC	RSV	VSS	NC	SDQ_B36	SDQ_B32	SDM_B4	VSS	SDQ_B48	SDQ_A39	VSS	SDQ_B43	VSS	VSS	SDQ_A42	SDQ_A47	VSS
AG	VSS	SDQS_B3	VSS	VSS	SCLK_B0#	SDQ_B33	NC	RSV	SDQ_A38	SDQ_B47	NC	SDQ_B46	SDQ_B42	SDQ_A46	RSV	SDM_A5	SDQS_A5
AH	SDQ_B30	VSS	SDQ_B31	VSS	SCLK_B0	NC	SDQS_B4	VSS	SDQ_A34	SDQS_B5	VSS	RSV	SDM_B5	VSS	VSS	SDQ_A40	SDQ_A41
AJ	VSS	SCB_B0	RSV	VSS	SCB_B2	SCB_B3	SDQ_B39	SDQ_B35	VSS	RSV	SDQ_B44	VSS	SDQ_B41	VSS	SDM_A4	SDQ_A45	VSS
AK	SDQ_B27	VSS	SDQS_B8	SCLK_B3#	VSS	NC	VSS	VSS	SDQS_A4	SCLK_A0	SDQ_A32	VSS	SDQ_A33	SDQ_B40	SDQ_B45	SDQ_A44	VCCSM
AL	VSS	SCB_B4	SCB_B6	SCB_B7	SCLK_B3	VSS	SDQ_B38	SDQ_B34	NC	SCLK_A0#	SCLK_A3#	SDQ_A36	SDQ_A37	VSS	SCS_A2#	SCAS_A#	SCS_A1#
AM	VCCSM	VCCSM	NC	VCCSM	VCCSM	NC	VCCSM	VCCSM	VCCSM	VSS	VCCSM	SCLK_A3	VSS	VCCSM	SCS_A0#	SCS_A3#	
AN	SMA_B0	SMA_A6	SMA_A3	SMA_A1	SMA_A0		NC	SBS_A1	SWE_B#	SBS_A0	NC	SWE_A#	NC	NC	SCS_B0#	SCS_B3#	VCCSM
AP	SMA_A5	VCCSM	SMA_A4	SMA_A2	RSV	VCCSM	NC	SBS_B0	SRAS_B#	VCCSM	SRAS_A#	NC	NC	NC	SCS_B2#	SCS_B1#	NC
AR	SBS_B1	SMA_B10	VSS	VCCSM	SMA_A10	RSV	VSS	VCCSM	SCAS_B#	NC	NC	VSS	VCCSM		VCCSM	NC	NC
	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

13.2 DDR2 Ballout Signal Lists

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 1 of 11)

DDR2 Signal Name	Ball
BSEL0	H16
BSEL1	E15
BSEL2	D17
CRTBLUE	H14
CRTBLUE#	J14
CRTDDCCLK	M15
CRTDDCDATA	L14
CRTGREEN	D14
CRTGREEN#	E14
CRTHSYNC	E12
CRTIREFSET	A15
CRTRED	F14
CRTRED#	G14
CRTVSYNC	D12
DMI_RXN0	U6
DMI_RXN1	T8
DMI_RXN2	V8
DMI_RXN3	U10
DMI_RXP0	U5
DMI_RXP1	T9
DMI_RXP2	V7
DMI_RXP3	V10
DMI_TXN0	T3
DMI_TXN1	U1
DMI_TXN2	V3
DMI_TXN3	W5
DMI_TXP0	R3
DMI_TXP1	T1
DMI_TXP2	U3
DMI_TXP3	V5
DREFCLKN	M12
DREFCLKP	M13
EXP_COMPI	W10
EXP_COMPO	Y10
EXP_RXN0	F11
EXP_RXN1	H11
EXP_RXN2	E9
EXP_RXN3	E7
EXP_RXN4	B4
EXP_RXN5	E5
EXP_RXN6	G5
EXP_RXN7	H7
EXP_RXP0	E11
EXP_RXP1	J11
EXP_RXP2	F9
EXP_RXP3	F7
EXP_RXP4	B3
EXP_RXP5	D5
EXP_RXP6	G6
EXP_RXP7	H8
EXP_TXN0	C9
EXP_TXN1	A8
EXP_TXN2	C7
EXP_TXN3	A6
EXP_TXN4	C5
EXP_TXN5	D2
EXP_TXN6	F3
EXP_TXN7	G1
EXP_TXP0	C10
EXP_TXP1	A9
EXP_TXP2	C8
EXP_TXP3	A7
EXP_TXP4	C6
EXP_TXP5	C2
EXP_TXP6	E3
EXP_TXP7	F1
EXTTS#	K16
GCLKN	B11
GCLKP	A11
HA10#	M30
HA11#	L31
HA12#	L28
HA13#	J28
HA14#	K27
HA15#	K33
HA16#	M28
HA17#	R29
HA18#	L26
HA19#	N26
HA20#	M26
HA21#	N31
HA22#	P26
HA23#	N29
HA24#	P28
HA25#	R28
HA26#	N33
HA27#	T27
HA28#	T31
HA29#	U28
HA3#	H29
HA30#	T26
HA31#	T29
HA4#	K29
HA5#	J29
HA6#	G30
HA7#	G32
HA8#	K30
HA9#	L29
HADS#	M31
HADSTB0#	J31
HADSTB1#	N27
HBNR#	M35
HBPRI#	E30
HBREQ0#	R33
HCLKN	M22
HCLKP	M23
HCPURST#	G24
HD0	J33
HD1	H33
HD10	D33
HD11	B34

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 2 of 11)

DDR2 Signal Name	Ball
HD12	C34
HD13	B33
HD14	C32
HD15	B32
HD16	E28
HD17	C30
HD18	D29
HD19	H28
HD2	J34
HD20	G29
HD21	J27
HD22	F28
HD23	F27
HD24	E27
HD25	E25
HD26	G25
HD27	J25
HD28	K25
HD29	L25
HD3	G35
HD30	L23
HD31	K23
HD32	J22
HD33	J24
HD34	K22
HD35	J21
HD36	M21
HD37	H23
HD38	M19
HD39	K21
HD4	H35
HD40	H20
HD41	H19
HD42	M18
HD43	K18
HD44	K17
HD45	G18
NC	AH24
NC	AH5

DDR2 Signal Name	Ball
HD46	H18
HD47	F17
HD48	A25
HD49	C27
HD5	G34
HD50	C31
HD51	B30
HD52	B31
HD53	A31
HD54	B27
HD55	A29
HD56	C28
HD57	A28
HD58	C25
HD59	C26
HD6	F34
HD60	D27
HD61	A27
HD62	E24
HD63	B25
HD7	G33
HD8	D34
HD9	C33
HDBSY#	L35
HDEFER#	J35
HDINV0#	E34
HDINV1#	J26
HDINV2#	K19
HDINV3#	B26
HDRDY#	M32
HDSTBN0#	E35
HDSTBN1#	F26
HDSTBN2#	F19
HDSTBN3#	C29
HDSTBP0#	E33
HDSTBP1#	H26
HDSTBP2#	J19
NC	R24
NC	T12

DDR2 Signal Name	Ball
HDSTBP3#	B29
HEDRDY#	P33
HHIT#	L34
HHITM#	N35
HLOCK#	L33
HPCREQ#	E31
HRCOMP	B23
HREQ0#	F33
HREQ1#	E32
HREQ2#	H31
HREQ3#	G31
HREQ4#	F31
HRS0#	K34
HRS1#	P34
HRS2#	J32
HSCOMP	D24
HSWING	A23
HTRDY#	N34
HVREF	A24
ICH_SYNC#	M14
MTYPE	C15
NC	A2
NC	A34
NC	A35
NC	AA12
NC	AB12
NC	AC23
NC	AC24
NC	AD21
NC	AD30
NC	AE18
NC	AE30
NC	AF19
NC	AF22
NC	AG25
NC	AG29
NC	AG6
RSV	H1
RSV	A16

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 3 of 11)

DDR2 Signal Name	Ball
NC	AJ14
NC	AK24
NC	AL27
NC	AM12
NC	AM15
NC	AM18
NC	AM21
NC	AM24
NC	AP1
NC	AP35
NC	AR1
NC	AR2
NC	AR34
NC	AR35
NC	B1
NC	B35
NC	C16
NC	E16
NC	F12
NC	F24
NC	G12
NC	H12
NC	H15
NC	H17
NC	J12
NC	K12
NC	L12
NC	L19
NC	N12
NC	N22
NC	N23
NC	N24
NC	P12
NC	P23
NC	P24
NC	P30
NC	R12
SCB_A3	AA30
SCB_A4	R30

DDR2 Signal Name	Ball
NC	U12
NC	V12
NC	W12
NC	Y12
PWROK	AG7
RSTIN#	AF7
RSV	L5
RSV	R10
RSV	M7
RSV	N5
RSV	P8
RSV	R5
RSV	J5
RSV	K7
RSV	L6
RSV	P10
RSV	M8
RSV	N6
RSV	P7
RSV	R6
RSV	J6
RSV	K8
RSV	K3
RSV	L1
RSV	M3
RSV	N1
RSV	P3
RSV	R1
RSV	H3
RSV	J1
RSV	J3
RSV	K1
RSV	L3
RSV	M1
RSV	N3
RSV	P1
RSV	G3
SCLK_B3	AL23
SCLK_B3#	AK22

DDR2 Signal Name	Ball
RSV	AC12
RSV	AC13
RSV	AC14
RSV	AC15
RSV	AC16
RSV	AC17
RSV	AC18
RSV	AC19
RSV	AC20
RSV	AC21
RSV	AC22
RSV	B15
RSV	C14
RSV	F15
RSV	G16
RSV	J13
RSV	K13
RSV	K15
RSV	M16
RSV	R35
RSV	AB33
RSV	AD32
RSV_TP0	AE16
RSV_TP1	AH15
RSV_TP2	AL15
RSV_TP3	AK15
SBS_A0	AN27
SBS_A1	AR27
SBS_A2	AR20
SBS_B0	AR16
SBS_B1	AN16
SBS_B2	AN9
SCAS_A#	AP29
SCAS_B#	AP18
SCB_A0	V32
SCB_A1	V31
SCB_A2	AA31
SDQ_A17	AK7
SDQ_A18	AM9

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 4 of 11)

DDR2 Signal Name	Ball
SCB_A5	R31
SCB_A6	Y30
SCB_A7	AB29
SCB_B0	AJ20
SCB_B1	AJ18
SCB_B2	AJ23
SCB_B3	AJ24
SCB_B4	AL20
SCB_B5	AK18
SCB_B6	AL21
SCB_B7	AL22
SCKE_A0	AP19
SCKE_A1	AN19
SCKE_A2	AN18
SCKE_A3	AR19
SCKE_B0	AR9
SCKE_B1	AP9
SCKE_B2	AR8
SCKE_B3	AN8
SCLK_A0	AL29
SCLK_A0#	AM30
SCLK_A1	AN2
SCLK_A1#	AN3
SCLK_A2	AC34
SCLK_A2#	AC35
SCLK_A3	AL28
SCLK_A3#	AK28
SCLK_A4	AM3
SCLK_A4#	AM2
SCLK_A5	AC33
SCLK_A5#	AB34
SCLK_B0	AH23
SCLK_B0#	AG23
SCLK_B1	AK9
SCLK_B1#	AL9
SCLK_B2	AE26
SCLK_B2#	AE25
SDQ_A52	AE35
SDQ_A53	AE34
SCLK_B4	AJ11
SCLK_B4#	AL11
SCLK_B5	AD28
SCLK_B5#	AD29
SCS_A0#	AR29
SCS_A1#	AN31
SCS_A2#	AR28
SCS_A3#	AP31
SCS_B0#	AP33
SCS_B1#	AM33
SCS_B2#	AN33
SCS_B3#	AP34
SDM_A0	AF2
SDM_A1	AL1
SDM_A2	AP6
SDM_A3	AF17
SDM_A4	AJ33
SDM_A5	AG34
SDM_A6	AA33
SDM_A7	U33
SDM_B0	AH10
SDM_B1	AK5
SDM_B2	AH12
SDM_B3	AE20
SDM_B4	AF25
SDM_B5	AH31
SDM_B6	AD24
SDM_B7	W31
SDQ_A0	AE3
SDQ_A1	AF3
SDQ_A10	AN4
SDQ_A11	AP4
SDQ_A12	AJ1
SDQ_A13	AJ3
SDQ_A14	AP2
SDQ_A15	AP3
SDQ_A16	AP5
SDQ_B3	AJ6
SDQ_B30	AH19
SDQ_A19	AL7
SDQ_A2	AH3
SDQ_A20	AR5
SDQ_A21	AN5
SDQ_A22	AM7
SDQ_A23	AM8
SDQ_A24	AE17
SDQ_A25	AF16
SDQ_A26	AL17
SDQ_A27	AH17
SDQ_A28	AE15
SDQ_A29	AD17
SDQ_A3	AJ2
SDQ_A30	AK16
SDQ_A31	AJ17
SDQ_A32	AK29
SDQ_A33	AK31
SDQ_A34	AH27
SDQ_A35	AD27
SDQ_A36	AL30
SDQ_A37	AL31
SDQ_A38	AG27
SDQ_A39	AF28
SDQ_A4	AE2
SDQ_A40	AH34
SDQ_A41	AH35
SDQ_A42	AF33
SDQ_A43	AE33
SDQ_A44	AK34
SDQ_A45	AJ34
SDQ_A46	AG32
SDQ_A47	AF34
SDQ_A48	AD31
SDQ_A49	AD35
SDQ_A5	AE1
SDQ_A50	Y33
SDQ_A51	W34
SDQ_B8	AK10
SDQ_B9	AL4

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 5 of 11)

DDR2 Signal Name	Ball
SDQ_A54	AA32
SDQ_A55	Y35
SDQ_A56	V34
SDQ_A57	V33
SDQ_A58	R32
SDQ_A59	R34
SDQ_A6	AG3
SDQ_A60	W35
SDQ_A61	W33
SDQ_A62	T33
SDQ_A63	T35
SDQ_A7	AH2
SDQ_A8	AK2
SDQ_A9	AK3
SDQ_B0	AG11
SDQ_B1	AG10
SDQ_B10	AL8
SDQ_B11	AF12
SDQ_B12	AH4
SDQ_B13	AJ5
SDQ_B14	AL6
SDQ_B15	AN6
SDQ_B16	AF13
SDQ_B17	AD14
SDQ_B18	AF14
SDQ_B19	AE14
SDQ_B2	AJ7
SDQ_B20	AD12
SDQ_B21	AE13
SDQ_B22	AK13
SDQ_B23	AL14
SDQ_B24	AD18
SDQ_B25	AE19
SDQ_B26	AL18
SDQ_B27	AK19
SDQ_B28	AF15
SDQ_B29	AD15
SMA_A1	AP25
SMA_A10	AP26

DDR2 Signal Name	Ball
SDQ_B31	AH21
SDQ_B32	AF24
SDQ_B33	AG24
SDQ_B34	AL26
SDQ_B35	AJ26
SDQ_B36	AF23
SDQ_B37	AD23
SDQ_B38	AL25
SDQ_B39	AJ25
SDQ_B4	AE11
SDQ_B40	AK32
SDQ_B41	AJ31
SDQ_B42	AG31
SDQ_B43	AF30
SDQ_B44	AJ29
SDQ_B45	AK33
SDQ_B46	AG30
SDQ_B47	AG28
SDQ_B48	AF27
SDQ_B49	AE27
SDQ_B5	AF11
SDQ_B50	AC26
SDQ_B51	AB26
SDQ_B52	AE31
SDQ_B53	AE29
SDQ_B54	AC28
SDQ_B55	AB27
SDQ_B56	AA28
SDQ_B57	W29
SDQ_B58	V28
SDQ_B59	V29
SDQ_B6	AJ8
SDQ_B60	Y26
SDQ_B61	AA29
SDQ_B62	W26
SDQ_B63	U26
SDQ_B7	AH7
SODT_B2	AL35
SODT_B3	AL33

DDR2 Signal Name	Ball
SDQS_A0	AG1
SDQS_A0#	AG2
SDQS_A1	AL3
SDQS_A1#	AL2
SDQS_A2	AP7
SDQS_A2#	AN7
SDQS_A3	AH16
SDQS_A3#	AG17
SDQS_A4	AK27
SDQS_A4#	AJ28
SDQS_A5	AG35
SDQS_A5#	AG33
SDQS_A6	AA34
SDQS_A6#	AA35
SDQS_A7	U34
SDQS_A7#	U35
SDQS_A8	V30
SDQS_A8#	U30
SDQS_B0	AH8
SDQS_B0#	AH9
SDQS_B1	AM5
SDQS_B1#	AL5
SDQS_B2	AH13
SDQS_B2#	AG14
SDQS_B3	AG20
SDQS_B3#	AF20
SDQS_B4	AH25
SDQS_B4#	AG26
SDQS_B5	AH28
SDQS_B5#	AH30
SDQS_B6	AB31
SDQS_B6#	AC30
SDQS_B7	W27
SDQS_B7#	Y28
SDQS_B8	AK21
SDQS_B8#	AJ21
SMA_A0	AN26
VCC	AB7
VCC	AB8

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 6 of 11)

DDR2 Signal Name	Ball
SMA_A11	AP21
SMA_A12	AN20
SMA_A13	AN30
SMA_A2	AN25
SMA_A3	AR24
SMA_A4	AP23
SMA_A5	AN22
SMA_A6	AR23
SMA_A7	AN21
SMA_A8	AN23
SMA_A9	AP22
SMA_B0	AN15
SMA_B1	AR15
SMA_B10	AP15
SMA_B11	AP10
SMA_B12	AN10
SMA_B13	AM34
SMA_B2	AN14
SMA_B3	AP14
SMA_B4	AN13
SMA_B5	AN11
SMA_B6	AP13
SMA_B7	AR11
SMA_B8	AR12
SMA_B9	AP11
SM_SLEWIN0	AJ12
SM_SLEWIN1	AF9
SM_SLEWOUT0	AK12
SM_SLEWOUT1	AE10
SOCOMP0	AF5
SOCOMP1	AE5
SODT_A0	AP30
SODT_A1	AP32
SODT_A2	AN29
SODT_A3	AN32
SODT_B0	AN34
SODT_B1	AL34
VCC	R13
VCC	R14

DDR2 Signal Name	Ball
SRAS_A#	AP27
SRAS_B#	AN17
SRCOMP0	AG4
SRCOMP1	AG8
SVREF0	AE7
SVREF1	AE8
SWE_A#	AN28
SWE_B#	AP17
VCC	AA13
VCC	AA14
VCC	AA16
VCC	AA18
VCC	AA20
VCC	AA21
VCC	AA22
VCC	AA23
VCC	AA24
VCC	AB1
VCC	AB10
VCC	AB11
VCC	AB13
VCC	AB14
VCC	AB15
VCC	AB16
VCC	AB17
VCC	AB18
VCC	AB19
VCC	AB2
VCC	AB20
VCC	AB21
VCC	AB22
VCC	AB23
VCC	AB24
VCC	AB3
VCC	AB4
VCC	AB5
VCC	AB6
VCC	W24
VCC	Y13

DDR2 Signal Name	Ball
VCC	AB9
VCC	AC1
VCC	AC10
VCC	AC11
VCC	AC2
VCC	AC3
VCC	AC4
VCC	AC5
VCC	AC6
VCC	AC7
VCC	AC8
VCC	AC9
VCC	AD1
VCC	AD10
VCC	AD2
VCC	AD3
VCC	AD4
VCC	AD5
VCC	AD6
VCC	AD7
VCC	AD8
VCC	AD9
VCC	L10
VCC	N13
VCC	N14
VCC	N15
VCC	N16
VCC	N18
VCC	N20
VCC	N21
VCC	P13
VCC	P14
VCC	P15
VCC	P17
VCC	P19
VCC	P21
VCC	P22
VCCSM	AM11
VCCSM	AM13

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 7 of 11)

DDR2 Signal Name	Ball
VCC	R15
VCC	R16
VCC	R18
VCC	R20
VCC	R22
VCC	R23
VCC	T13
VCC	T14
VCC	T15
VCC	T16
VCC	T17
VCC	T19
VCC	T20
VCC	T21
VCC	T23
VCC	T24
VCC	U13
VCC	U14
VCC	U16
VCC	U18
VCC	U20
VCC	U22
VCC	U24
VCC	V13
VCC	V14
VCC	V15
VCC	V17
VCC	V19
VCC	V21
VCC	V23
VCC	V24
VCC	W13
VCC	W14
VCC	W16
VCC	W18
VCC	W20
VCC	W22
VSS	AA15
VSS	AA17

DDR2 Signal Name	Ball
VCC	Y14
VCC	Y15
VCC	Y16
VCC	Y17
VCC	Y19
VCC	Y20
VCC	Y21
VCC	Y23
VCC	Y24
VCC_EXP	W1
VCC_EXP	W2
VCC_EXP	W3
VCC_EXP	W4
VCC_EXP	W6
VCC_EXP	W7
VCC_EXP	W8
VCC_EXP	W9
VCC_EXP	Y1
VCC_EXP	Y2
VCC_EXP	Y3
VCC_EXP	Y4
VCC_EXP	Y5
VCC_EXP	Y6
VCC_EXP	Y7
VCC_EXP	Y8
VCC_EXP	Y9
VCC2	A13
VCCA_DAC	D13
VCCA_DAC	E13
VCCA_DPLLA	A12
VCCA_DPLLB	B13
VCCA_EXPPLL	A14
VCCA_HPLL	A17
VCCA_SMPLL	B17
VCCSM	AK35
VCCSM	AL12
VCCSM	AM10
VSS	AE32
VSS	AE4

DDR2 Signal Name	Ball
VCCSM	AM14
VCCSM	AM16
VCCSM	AM17
VCCSM	AM19
VCCSM	AM20
VCCSM	AM22
VCCSM	AM23
VCCSM	AM25
VCCSM	AM26
VCCSM	AM27
VCCSM	AM29
VCCSM	AM32
VCCSM	AN35
VCCSM	AP12
VCCSM	AP16
VCCSM	AP20
VCCSM	AP24
VCCSM	AP28
VCCSM	AP8
VCCSM	AR10
VCCSM	AR14
VCCSM	AR18
VCCSM	AR22
VCCSM	AR26
VCCSM	AR31
VCCSM	AR33
VCCSM	AR7
VSS	A10
VSS	A18
VSS	A26
VSS	A3
VSS	A30
VSS	A33
VSS	A5
VSS	AA1
VSS	AA10
VSS	AA11
VSS	AJ15
VSS	AJ16

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 8 of 11)

DDR2 Signal Name	Ball
VSS	AA19
VSS	AA2
VSS	AA25
VSS	AA26
VSS	AA27
VSS	AA3
VSS	AA4
VSS	AA5
VSS	AA6
VSS	AA7
VSS	AA8
VSS	AA9
VSS	AB25
VSS	AB28
VSS	AB30
VSS	AB32
VSS	AB35
VSS	AC25
VSS	AC27
VSS	AC29
VSS	AC31
VSS	AC32
VSS	AD11
VSS	AD13
VSS	AD16
VSS	AD19
VSS	AD20
VSS	AD22
VSS	AD25
VSS	AD26
VSS	AD34
VSS	AE12
VSS	AE21
VSS	AE22
VSS	AE23
VSS	AE24
VSS	AE28
VSS	AR6
VSS	B10

DDR2 Signal Name	Ball
VSS	AE6
VSS	AE9
VSS	AF1
VSS	AF10
VSS	AF18
VSS	AF21
VSS	AF26
VSS	AF29
VSS	AF31
VSS	AF32
VSS	AF35
VSS	AF4
VSS	AF6
VSS	AF8
VSS	AG12
VSS	AG13
VSS	AG15
VSS	AG16
VSS	AG18
VSS	AG19
VSS	AG21
VSS	AG22
VSS	AG5
VSS	AG9
VSS	AH1
VSS	AH11
VSS	AH14
VSS	AH18
VSS	AH20
VSS	AH22
VSS	AH26
VSS	AH29
VSS	AH32
VSS	AH33
VSS	AH6
VSS	AJ10
VSS	AJ13
VSS	D8
VSS	D9

DDR2 Signal Name	Ball
VSS	AJ19
VSS	AJ22
VSS	AJ27
VSS	AJ30
VSS	AJ32
VSS	AJ35
VSS	AJ4
VSS	AJ9
VSS	AK1
VSS	AK11
VSS	AK14
VSS	AK17
VSS	AK20
VSS	AK23
VSS	AK25
VSS	AK26
VSS	AK30
VSS	AK4
VSS	AK6
VSS	AK8
VSS	AL10
VSS	AL13
VSS	AL16
VSS	AL19
VSS	AL24
VSS	AL32
VSS	AM28
VSS	AM31
VSS	AM4
VSS	AM6
VSS	AN1
VSS	AR13
VSS	AR17
VSS	AR21
VSS	AR25
VSS	AR3
VSS	AR30
VSS	G4
VSS	G7

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 9 of 11)

DDR2 Signal Name	Ball
VSS	B12
VSS	B14
VSS	B16
VSS	B18
VSS	B2
VSS	B24
VSS	B28
VSS	B5
VSS	B6
VSS	B7
VSS	B8
VSS	B9
VSS	C1
VSS	C11
VSS	C13
VSS	C17
VSS	C18
VSS	C23
VSS	C3
VSS	C35
VSS	C4
VSS	D10
VSS	D11
VSS	D15
VSS	D16
VSS	D18
VSS	D23
VSS	D25
VSS	D26
VSS	D28
VSS	D3
VSS	D30
VSS	D31
VSS	D32
VSS	D4
VSS	D6
VSS	D7
VSS	K31
VSS	K32

DDR2 Signal Name	Ball
VSS	E1
VSS	E10
VSS	E17
VSS	E18
VSS	E2
VSS	E23
VSS	E26
VSS	E29
VSS	E4
VSS	E6
VSS	E8
VSS	F10
VSS	F16
VSS	F18
VSS	F2
VSS	F23
VSS	F25
VSS	F29
VSS	F30
VSS	F32
VSS	F35
VSS	F4
VSS	F5
VSS	F6
VSS	F8
VSS	G10
VSS	G11
VSS	G13
VSS	G15
VSS	G17
VSS	G19
VSS	G2
VSS	G20
VSS	G23
VSS	G26
VSS	G27
VSS	G28
VSS	N10
VSS	N11

DDR2 Signal Name	Ball
VSS	G8
VSS	G9
VSS	H10
VSS	H13
VSS	H2
VSS	H21
VSS	H24
VSS	H25
VSS	H27
VSS	H30
VSS	H32
VSS	H34
VSS	H4
VSS	H5
VSS	H6
VSS	H9
VSS	J10
VSS	J15
VSS	J16
VSS	J17
VSS	J18
VSS	J2
VSS	J20
VSS	J23
VSS	J30
VSS	J4
VSS	J7
VSS	J8
VSS	J9
VSS	K10
VSS	K11
VSS	K14
VSS	K2
VSS	K20
VSS	K24
VSS	K26
VSS	K28
VSS	R9
VSS	T10

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 10 of 11)

DDR2 Signal Name	Ball
VSS	K35
VSS	K4
VSS	K5
VSS	K6
VSS	K9
VSS	L11
VSS	L13
VSS	L15
VSS	L16
VSS	L17
VSS	L18
VSS	L2
VSS	L20
VSS	L21
VSS	L22
VSS	L24
VSS	L27
VSS	L30
VSS	L32
VSS	L4
VSS	L7
VSS	L8
VSS	L9
VSS	M10
VSS	M11
VSS	M17
VSS	M2
VSS	M20
VSS	M24
VSS	M25
VSS	M27
VSS	M29
VSS	M34
VSS	M4
VSS	M5
VSS	M6
VSS	M9
VSS	V26
VSS	V27

DDR2 Signal Name	Ball
VSS	N17
VSS	N19
VSS	N2
VSS	N25
VSS	N28
VSS	N30
VSS	N32
VSS	N4
VSS	N7
VSS	N8
VSS	N9
VSS	P11
VSS	P16
VSS	P18
VSS	P2
VSS	P20
VSS	P25
VSS	P27
VSS	P29
VSS	P31
VSS	P32
VSS	P35
VSS	P4
VSS	P5
VSS	P6
VSS	P9
VSS	R11
VSS	R17
VSS	R19
VSS	R2
VSS	R21
VSS	R25
VSS	R26
VSS	R27
VSS	R4
VSS	R7
VSS	R8
VSS	Y22
VSS	Y25

DDR2 Signal Name	Ball
VSS	T11
VSS	T18
VSS	T2
VSS	T22
VSS	T25
VSS	T28
VSS	T30
VSS	T32
VSS	T34
VSS	T4
VSS	T5
VSS	T6
VSS	T7
VSS	U11
VSS	U15
VSS	U17
VSS	U19
VSS	U2
VSS	U21
VSS	U23
VSS	U25
VSS	U27
VSS	U29
VSS	U31
VSS	U32
VSS	U4
VSS	U7
VSS	U8
VSS	U9
VSS	V1
VSS	V11
VSS	V16
VSS	V18
VSS	V2
VSS	V20
VSS	V22
VSS	V25
VTT	C20
VTT	C21

Table 13-1. Intel® E7221 MCH DDR2 Signal List by Name (Sheet 11 of 11)

DDR2 Signal Name	Ball
VSS	V35
VSS	V4
VSS	V6
VSS	V9
VSS	W11
VSS	W15
VSS	W17
VSS	W19
VSS	W21
VSS	W23
VSS	W25
VSS	W28
VSS	W30
VSS	W32
VSS	Y11
VSS	Y18

DDR2 Signal Name	Ball
VSS	Y27
VSS	Y29
VSS	Y31
VSS	Y32
VSS	Y34
VSSA_DAC	F13
VTT	A19
VTT	A20
VTT	A21
VTT	A22
VTT	B19
VTT	B20
VTT	B21
VTT	B22
VTT	C19

DDR2 Signal Name	Ball
VTT	C22
VTT	D19
VTT	D20
VTT	D21
VTT	D22
VTT	E19
VTT	E20
VTT	E21
VTT	E22
VTT	F20
VTT	F21
VTT	F22
VTT	G21
VTT	G22
VTT	H22

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 1 of 11)

Ball	DDR2 Signal Name
A1	----
A2	NC
A3	VSS
A4	----
A5	VSS
A6	EXP_TXN3
A7	EXP_TXP3
A8	EXP_TXN1
A9	EXP_TXP1
A10	VSS
A11	GCLKP
A12	VCCA_DPLLA
A13	VCC2
A14	VCCA_EXPPLL
A15	CRTIREFSET
A16	RSV
A17	VCCA_HPLL
A18	VSS
A19	VTT
A20	VTT
A21	VTT
A22	VTT
A23	HSWING
A24	HVREF
A25	HD48
A26	VSS
A27	HD61
A28	HD57
A29	HD55
A30	VSS
A31	HD53
A32	----
A33	VSS
A34	NC
A35	NC
B1	NC
B2	VSS
B3	EXP_RXP4

Ball	DDR2 Signal Name
B4	EXP_RXN4
B5	VSS
B6	VSS
B7	VSS
B8	VSS
B9	VSS
B10	VSS
B11	GCLKN
B12	VSS
B13	VCCA_DPLLB
B14	VSS
B15	RSV
B16	VSS
B17	VCCA_SMPLL
B18	VSS
B19	VTT
B20	VTT
B21	VTT
B22	VTT
B23	HRCOMP
B24	VSS
B25	HD63
B26	HDINV3#
B27	HD54
B28	VSS
B29	HDSTBP3#
B30	HD51
B31	HD52
B32	HD15
B33	HD13
B34	HD11
B35	NC
C1	VSS
C2	EXP_TXP5
C3	VSS
C4	VSS
C5	EXP_TXN4
C6	EXP_TXP4

Ball	DDR2 Signal Name
C7	EXP_TXN2
C8	EXP_TXP2
C9	EXP_TXN0
C10	EXP_TXP0
C11	VSS
C12	----
C13	VSS
C14	RSV
C15	MTYPE
C16	NC
C17	VSS
C18	VSS
C19	VTT
C20	VTT
C21	VTT
C22	VTT
C23	VSS
C24	----
C25	HD58
C26	HD59
C27	HD49
C28	HD56
C29	HDSTBN3#
C30	HD17
C31	HD50
C32	HD14
C33	HD9
C34	HD12
C35	VSS
D1	----
D2	EXP_TXN5
D3	VSS
D4	VSS
D5	EXP_RXP5
D6	VSS
D7	VSS
D8	VSS
D9	VSS

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 2 of 11)

Ball	DDR2 Signal Name
D10	VSS
D11	VSS
D12	CRTVSYNC
D13	VCCA_DAC
D14	CRTGREEN
D15	VSS
D16	VSS
D17	BSEL2
D18	VSS
D19	VTT
D20	VTT
D21	VTT
D22	VTT
D23	VSS
D24	HSCOMP
D25	VSS
D26	VSS
D27	HD60
D28	VSS
D29	HD18
D30	VSS
D31	VSS
D32	VSS
D33	HD10
D34	HD8
D35	----
E1	VSS
E2	VSS
E3	EXP_TXP6
E4	VSS
E5	EXP_RXN5
E6	VSS
E7	EXP_RXN3
E8	VSS
E9	EXP_RXN2
E10	VSS
E11	EXP_RXP0
E12	CRTHSYNC
E13	VCCA_DAC

Ball	DDR2 Signal Name
E14	CRTGREEN#
E15	BSEL1
E16	NC
E17	VSS
E18	VSS
E19	VTT
E20	VTT
E21	VTT
E22	VTT
E23	VSS
E24	HD62
E25	HD25
E26	VSS
E27	HD24
E28	HD16
E29	VSS
E30	HBPRI#
E31	HPCREQ#
E32	HREQ1#
E33	HDSTBP0#
E34	HDINV0#
E35	HDSTBN0#
F1	EXP_TXP7
F2	VSS
F3	EXP_TXN6
F4	VSS
F5	VSS
F6	VSS
F7	EXP_RXP3
F8	VSS
F9	EXP_RXP2
F10	VSS
F11	EXP_RXN0
F12	NC
F13	VSSA_DAC
F14	CRTRED
F15	RSV
F16	VSS
F17	HD47

Ball	DDR2 Signal Name
F18	VSS
F19	HDSTBN2#
F20	VTT
F21	VTT
F22	VTT
F23	VSS
F24	NC
F25	VSS
F26	HDSTBN1#
F27	HD23
F28	HD22
F29	VSS
F30	VSS
F31	HREQ4#
F32	VSS
F33	HREQ0#
F34	HD6
F35	VSS
G1	EXP_TXN7
G2	VSS
G3	RSV
G4	VSS
G5	EXP_RXN6
G6	EXP_RXP6
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	VSS
G12	NC
G13	VSS
G14	CRTRED#
G15	VSS
G16	RSV
G17	VSS
G18	HD45
G19	VSS
G20	VSS
G21	VTT

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 3 of 11)

Ball	DDR2 Signal Name
G22	VTT
G23	VSS
G24	HCPURST#
G25	HD26
G26	VSS
G27	VSS
G28	VSS
G29	HD20
G30	HA6#
G31	HREQ3#
G32	HA7#
G33	HD7
G34	HD5
G35	HD3
H1	RSV
H2	VSS
H3	RSV
H4	VSS
H5	VSS
H6	VSS
H7	EXP_RXN7
H8	EXP_RXP7
H9	VSS
H10	VSS
H11	EXP_RXN1
H12	NC
H13	VSS
H14	CRTBLUE
H15	NC
H16	BSEL0
H17	NC
H18	HD46
H19	HD41
H20	HD40
H21	VSS
H22	VTT
H23	HD37
H24	VSS
H25	VSS

Ball	DDR2 Signal Name
H26	HDSTBP1#
H27	VSS
H28	HD19
H29	HA3#
H30	VSS
H31	HREQ2#
H32	VSS
H33	HD1
H34	VSS
H35	HD4
J1	RSV
J2	VSS
J3	RSV
J4	VSS
J5	RSV
J6	RSV
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	EXP_RXP1
J12	NC
J13	RSV
J14	CRTBLUE#
J15	VSS
J16	VSS
J17	VSS
J18	VSS
J19	HDSTBP2#
J20	VSS
J21	HD35
J22	HD32
J23	VSS
J24	HD33
J25	HD27
J26	HDINV1#
J27	HD21
J28	HA13#
J29	HA5#

Ball	DDR2 Signal Name
J30	VSS
J31	HADSTB0#
J32	HRS2#
J33	HD0
J34	HD2
J35	HDEFER#
K1	RSV
K2	VSS
K3	RSV
K4	VSS
K5	VSS
K6	VSS
K7	RSV
K8	RSV
K9	VSS
K10	VSS
K11	VSS
K12	NC
K13	RSV
K14	VSS
K15	RSV
K16	EXTTS#
K17	HD44
K18	HD43
K19	HDINV2#
K20	VSS
K21	HD39
K22	HD34
K23	HD31
K24	VSS
K25	HD28
K26	VSS
K27	HA14#
K28	VSS
K29	HA4#
K30	HA8#
K31	VSS
K32	VSS
K33	HA15#

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 4 of 11)

Ball	DDR2 Signal Name
K34	HRS0#
K35	VSS
L1	RSV
L2	VSS
L3	RSV
L4	VSS
L5	RSV
L6	RSV
L7	VSS
L8	VSS
L9	VSS
L10	VCC
L11	VSS
L12	NC
L13	VSS
L14	CRTDDCDATA
L15	VSS
L16	VSS
L17	VSS
L18	VSS
L19	NC
L20	VSS
L21	VSS
L22	VSS
L23	HD30
L24	VSS
L25	HD29
L26	HA18#
L27	VSS
L28	HA12#
L29	HA9#
L30	VSS
L31	HA11#
L32	VSS
L33	HLOCK#
L34	HHIT#
L35	HDBSY#
M1	RSV
M2	VSS

Ball	DDR2 Signal Name
M3	RSV
M4	VSS
M5	VSS
M6	VSS
M7	RSV
M8	RSV
M9	VSS
M10	VSS
M11	VSS
M12	DREFCLKN
M13	DREFCLKP
M14	ICH_SYNC#
M15	CRTDDCCLK
M16	RSV
M17	VSS
M18	HD42
M19	HD38
M20	VSS
M21	HD36
M22	HCLKN
M23	HCLKP
M24	VSS
M25	VSS
M26	HA20#
M27	VSS
M28	HA16#
M29	VSS
M30	HA10#
M31	HADS#
M32	HDRDY#
M33	----
M34	VSS
M35	HBNR#
N1	RSV
N2	VSS
N3	RSV
N4	VSS
N5	RSV
N6	RSV

Ball	DDR2 Signal Name
N7	VSS
N8	VSS
N9	VSS
N10	VSS
N11	VSS
N12	NC
N13	VCC
N14	VCC
N15	VCC
N16	VCC
N17	VSS
N18	VCC
N19	VSS
N20	VCC
N21	VCC
N22	NC
N23	NC
N24	NC
N25	VSS
N26	HA19#
N27	HADSTB1#
N28	VSS
N29	HA23#
N30	VSS
N31	HA21#
N32	VSS
N33	HA26#
N34	HTRDY#
N35	HHITM#
P1	RSV
P2	VSS
P3	RSV
P4	VSS
P5	VSS
P6	VSS
P7	RSV
P8	RSV
P9	VSS
P10	RSV

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 5 of 11)

Ball	DDR2 Signal Name
P11	VSS
P12	NC
P13	VCC
P14	VCC
P15	VCC
P16	VSS
P17	VCC
P18	VSS
P19	VCC
P20	VSS
P21	VCC
P22	VCC
P23	NC
P24	NC
P25	VSS
P26	HA22#
P27	VSS
P28	HA24#
P29	VSS
P30	NC
P31	VSS
P32	VSS
P33	HEDRDY#
P34	HRS1#
P35	VSS
R1	RSV
R2	VSS
R3	DMI_TXP0
R4	VSS
R5	RSV
R6	RSV
R7	VSS
R8	VSS
R9	VSS
R10	RSV
R11	VSS
R12	NC
R13	VCC
R14	VCC
R15	VCC
R16	VCC
R17	VSS
R18	VCC
R19	VSS
R20	VCC
R21	VSS
R22	VCC
R23	VCC
R24	NC
R25	VSS
R26	VSS
R27	VSS
R28	HA25#
R29	HA17#
R30	SCB_A4
R31	SCB_A5
R32	SDQ_A58
R33	HBREQ0#
R34	SDQ_A59
R35	RSV
T1	DMI_TXP1
T2	VSS
T3	DMI_TXN0
T4	VSS
T5	VSS
T6	VSS
T7	VSS
T8	DMI_RXN1
T9	DMI_RXP1
T10	VSS
T11	VSS
T12	NC
T13	VCC
T14	VCC
T15	VCC
T16	VCC
T17	VCC
T18	VSS
T19	VCC
T20	VCC
T21	VCC
T22	VSS
T23	VCC
T24	VCC
T25	VSS
T26	HA30#
T27	HA27#
T28	VSS
T29	HA31#
T30	VSS
T31	HA28#
T32	VSS
T33	SDQ_A62
T34	VSS
T35	SDQ_A63
U1	DMI_TXN1
U2	VSS
U3	DMI_TXP2
U4	VSS
U5	DMI_RXP0
U6	DMI_RXN0
U7	VSS
U8	VSS
U9	VSS
U10	DMI_RXN3
U11	VSS
U12	NC
U13	VCC
U14	VCC
U15	VSS
U16	VCC
U17	VSS
U18	VCC
U19	VSS
U20	VCC
U21	VSS
U22	VCC

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 6 of 11)

Ball	DDR2 Signal Name
U23	VSS
U24	VCC
U25	VSS
U26	SDQ_B63
U27	VSS
U28	HA29#
U29	VSS
U30	SDQS_A8#
U31	VSS
U32	VSS
U33	SDM_A7
U34	SDQS_A7
U35	SDQS_A7#
V1	VSS
V2	VSS
V3	DMI_TXN2
V4	VSS
V5	DMI_TXP3
V6	VSS
V7	DMI_RXP2
V8	DMI_RXN2
V9	VSS
V10	DMI_RXP3
V11	VSS
V12	NC
V13	VCC
V14	VCC
V15	VCC
V16	VSS
V17	VCC
V18	VSS
V19	VCC
V20	VSS
V21	VCC
V22	VSS
V23	VCC
V24	VCC
V25	VSS
V26	VSS

Ball	DDR2 Signal Name
V27	VSS
V28	SDQ_B58
V29	SDQ_B59
V30	SDQS_A8
V31	SCB_A1
V32	SCB_A0
V33	SDQ_A57
V34	SDQ_A56
V35	VSS
W1	VCC_EXP
W2	VCC_EXP
W3	VCC_EXP
W4	VCC_EXP
W5	DMI_TXN3
W6	VCC_EXP
W7	VCC_EXP
W8	VCC_EXP
W9	VCC_EXP
W10	EXP_COMPI
W11	VSS
W12	NC
W13	VCC
W14	VCC
W15	VSS
W16	VCC
W17	VSS
W18	VCC
W19	VSS
W20	VCC
W21	VSS
W22	VCC
W23	VSS
W24	VCC
W25	VSS
W26	SDQ_B62
W27	SDQS_B7
W28	VSS
W29	SDQ_B57
W30	VSS

Ball	DDR2 Signal Name
W31	SDM_B7
W32	VSS
W33	SDQ_A61
W34	SDQ_A51
W35	SDQ_A60
Y1	VCC_EXP
Y2	VCC_EXP
Y3	VCC_EXP
Y4	VCC_EXP
Y5	VCC_EXP
Y6	VCC_EXP
Y7	VCC_EXP
Y8	VCC_EXP
Y9	VCC_EXP
Y10	EXP_COMPO
Y11	VSS
Y12	NC
Y13	VCC
Y14	VCC
Y15	VCC
Y16	VCC
Y17	VCC
Y18	VSS
Y19	VCC
Y20	VCC
Y21	VCC
Y22	VSS
Y23	VCC
Y24	VCC
Y25	VSS
Y26	SDQ_B60
Y27	VSS
Y28	SDQS_B7#
Y29	VSS
Y30	SCB_A6
Y31	VSS
Y32	VSS
Y33	SDQ_A50
Y34	VSS

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 7 of 11)

Ball	DDR2 Signal Name
Y35	SDQ_A55
AA1	VSS
AA2	VSS
AA3	VSS
AA4	VSS
AA5	VSS
AA6	VSS
AA7	VSS
AA8	VSS
AA9	VSS
AA10	VSS
AA11	VSS
AA12	NC
AA13	VCC
AA14	VCC
AA15	VSS
AA16	VCC
AA17	VSS
AA18	VCC
AA19	VSS
AA20	VCC
AA21	VCC
AA22	VCC
AA23	VCC
AA24	VCC
AA25	VSS
AA26	VSS
AA27	VSS
AA28	SDQ_B56
AA29	SDQ_B61
AA30	SCB_A3
AA31	SCB_A2
AA32	SDQ_A54
AA33	SDM_A6
AA34	SDQS_A6
AA35	SDQS_A6#
AB1	VCC
AB2	VCC
AB3	VCC

Ball	DDR2 Signal Name
AB4	VCC
AB5	VCC
AB6	VCC
AB7	VCC
AB8	VCC
AB9	VCC
AB10	VCC
AB11	VCC
AB12	NC
AB13	VCC
AB14	VCC
AB15	VCC
AB16	VCC
AB17	VCC
AB18	VCC
AB19	VCC
AB20	VCC
AB21	VCC
AB22	VCC
AB23	VCC
AB24	VCC
AB25	VSS
AB26	SDQ_B51
AB27	SDQ_B55
AB28	VSS
AB29	SCB_A7
AB30	VSS
AB31	SDQS_B6
AB32	VSS
AB33	RSV
AB34	SCLK_A5#
AB35	VSS
AC1	VCC
AC2	VCC
AC3	VCC
AC4	VCC
AC5	VCC
AC6	VCC
AC7	VCC

Ball	DDR2 Signal Name
AC8	VCC
AC9	VCC
AC10	VCC
AC11	VCC
AC12	RSV
AC13	RSV
AC14	RSV
AC15	RSV
AC16	RSV
AC17	RSV
AC18	RSV
AC19	RSV
AC20	RSV
AC21	RSV
AC22	RSV
AC23	NC
AC24	NC
AC25	VSS
AC26	SDQ_B50
AC27	VSS
AC28	SDQ_B54
AC29	VSS
AC30	SDQS_B6#
AC31	VSS
AC32	VSS
AC33	SCLK_A5
AC34	SCLK_A2
AC35	SCLK_A2#
AD1	VCC
AD2	VCC
AD3	VCC
AD4	VCC
AD5	VCC
AD6	VCC
AD7	VCC
AD8	VCC
AD9	VCC
AD10	VCC
AD11	VSS

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 8 of 11)

Ball	DDR2 Signal Name
AD12	SDQ_B20
AD13	VSS
AD14	SDQ_B17
AD15	SDQ_B29
AD16	VSS
AD17	SDQ_A29
AD18	SDQ_B24
AD19	VSS
AD20	VSS
AD21	NC
AD22	VSS
AD23	SDQ_B37
AD24	SDM_B6
AD25	VSS
AD26	VSS
AD27	SDQ_A35
AD28	SCLK_B5
AD29	SCLK_B5#
AD30	NC
AD31	SDQ_A48
AD32	RSV
AD33	----
AD34	VSS
AD35	SDQ_A49
AE1	SDQ_A5
AE2	SDQ_A4
AE3	SDQ_A0
AE4	VSS
AE5	SOCOMP1
AE6	VSS
AE7	SVREF0
AE8	SVREF1
AE9	VSS
AE10	SM_SLEWOUT1
AE11	SDQ_B4
AE12	VSS
AE13	SDQ_B21
AE14	SDQ_B19
AE15	SDQ_A28

Ball	DDR2 Signal Name
AE16	RSV_TP0
AE17	SDQ_A24
AE18	NC
AE19	SDQ_B25
AE20	SDM_B3
AE21	VSS
AE22	VSS
AE23	VSS
AE24	VSS
AE25	SCLK_B2#
AE26	SCLK_B2
AE27	SDQ_B49
AE28	VSS
AE29	SDQ_B53
AE30	NC
AE31	SDQ_B52
AE32	VSS
AE33	SDQ_A43
AE34	SDQ_A53
AE35	SDQ_A52
AF1	VSS
AF2	SDM_A0
AF3	SDQ_A1
AF4	VSS
AF5	SOCOMP0
AF6	VSS
AF7	RSTIN#
AF8	VSS
AF9	SM_SLEWIN1
AF10	VSS
AF11	SDQ_B5
AF12	SDQ_B11
AF13	SDQ_B16
AF14	SDQ_B18
AF15	SDQ_B28
AF16	SDQ_A25
AF17	SDM_A3
AF18	VSS
AF19	NC

Ball	DDR2 Signal Name
AF20	SDQS_B3#
AF21	VSS
AF22	NC
AF23	SDQ_B36
AF24	SDQ_B32
AF25	SDM_B4
AF26	VSS
AF27	SDQ_B48
AF28	SDQ_A39
AF29	VSS
AF30	SDQ_B43
AF31	VSS
AF32	VSS
AF33	SDQ_A42
AF34	SDQ_A47
AF35	VSS
AG1	SDQS_A0
AG2	SDQS_A0#
AG3	SDQ_A6
AG4	SRCOMP0
AG5	VSS
AG6	NC
AG7	PWROK
AG8	SRCOMP1
AG9	VSS
AG10	SDQ_B1
AG11	SDQ_B0
AG12	VSS
AG13	VSS
AG14	SDQS_B2#
AG15	VSS
AG16	VSS
AG17	SDQS_A3#
AG18	VSS
AG19	VSS
AG20	SDQS_B3
AG21	VSS
AG22	VSS
AG23	SCLK_B0#

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 9 of 11)

Ball	DDR2 Signal Name
AG24	SDQ_B33
AG25	NC
AG26	SDQS_B4#
AG27	SDQ_A38
AG28	SDQ_B47
AG29	NC
AG30	SDQ_B46
AG31	SDQ_B42
AG32	SDQ_A46
AG33	SDQS_A5#
AG34	SDM_A5
AG35	SDQS_A5
AH1	VSS
AH2	SDQ_A7
AH3	SDQ_A2
AH4	SDQ_B12
AH5	NC
AH6	VSS
AH7	SDQ_B7
AH8	SDQS_B0
AH9	SDQS_B0#
AH10	SDM_B0
AH11	VSS
AH12	SDM_B2
AH13	SDQS_B2
AH14	VSS
AH15	RSV_TP1
AH16	SDQS_A3
AH17	SDQ_A27
AH18	VSS
AH19	SDQ_B30
AH20	VSS
AH21	SDQ_B31
AH22	VSS
AH23	SCLK_B0
AH24	NC
AH25	SDQS_B4
AH26	VSS
AH27	SDQ_A34
AH28	SDQS_B5
AH29	VSS
AH30	SDQS_B5#
AH31	SDM_B5
AH32	VSS
AH33	VSS
AH34	SDQ_A40
AH35	SDQ_A41
AJ1	SDQ_A12
AJ2	SDQ_A3
AJ3	SDQ_A13
AJ4	VSS
AJ5	SDQ_B13
AJ6	SDQ_B3
AJ7	SDQ_B2
AJ8	SDQ_B6
AJ9	VSS
AJ10	VSS
AJ11	SCLK_B4
AJ12	SM_SLEWIN0
AJ13	VSS
AJ14	NC
AJ15	VSS
AJ16	VSS
AJ17	SDQ_A31
AJ18	SCB_B1
AJ19	VSS
AJ20	SCB_B0
AJ21	SDQS_B8#
AJ22	VSS
AJ23	SCB_B2
AJ24	SCB_B3
AJ25	SDQ_B39
AJ26	SDQ_B35
AJ27	VSS
AJ28	SDQS_A4#
AJ29	SDQ_B44
AJ30	VSS
AJ31	SDQ_B41
AJ32	VSS
AJ33	SDM_A4
AJ34	SDQ_A45
AJ35	VSS
AK1	VSS
AK2	SDQ_A8
AK3	SDQ_A9
AK4	VSS
AK5	SDM_B1
AK6	VSS
AK7	SDQ_A17
AK8	VSS
AK9	SCLK_B1
AK10	SDQ_B8
AK11	VSS
AK12	SM_SLEWOUT0
AK13	SDQ_B22
AK14	VSS
AK15	RSV_TP3
AK16	SDQ_A30
AK17	VSS
AK18	SCB_B5
AK19	SDQ_B27
AK20	VSS
AK21	SDQS_B8
AK22	SCLK_B3#
AK23	VSS
AK24	NC
AK25	VSS
AK26	VSS
AK27	SDQS_A4
AK28	SCLK_A3#
AK29	SDQ_A32
AK30	VSS
AK31	SDQ_A33
AK32	SDQ_B40
AK33	SDQ_B45
AK34	SDQ_A44
AK35	VCCSM

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 10 of 11)

Ball	DDR2 Signal Name
AL1	SDM_A1
AL2	SDQS_A1#
AL3	SDQS_A1
AL4	SDQ_B9
AL5	SDQS_B1#
AL6	SDQ_B14
AL7	SDQ_A19
AL8	SDQ_B10
AL9	SCLK_B1#
AL10	VSS
AL11	SCLK_B4#
AL12	VCCSM
AL13	VSS
AL14	SDQ_B23
AL15	RSV_TP2
AL16	VSS
AL17	SDQ_A26
AL18	SDQ_B26
AL19	VSS
AL20	SCB_B4
AL21	SCB_B6
AL22	SCB_B7
AL23	SCLK_B3
AL24	VSS
AL25	SDQ_B38
AL26	SDQ_B34
AL27	NC
AL28	SCLK_A3
AL29	SCLK_A0
AL30	SDQ_A36
AL31	SDQ_A37
AL32	VSS
AL33	SODT_B3
AL34	SODT_B1
AL35	SODT_B2
AM1	----
AM2	SCLK_A4#
AM3	SCLK_A4
AM4	VSS

Ball	DDR2 Signal Name
AM5	SDQS_B1
AM6	VSS
AM7	SDQ_A22
AM8	SDQ_A23
AM9	SDQ_A18
AM10	VCCSM
AM11	VCCSM
AM12	NC
AM13	VCCSM
AM14	VCCSM
AM15	NC
AM16	VCCSM
AM17	VCCSM
AM18	NC
AM19	VCCSM
AM20	VCCSM
AM21	NC
AM22	VCCSM
AM23	VCCSM
AM24	NC
AM25	VCCSM
AM26	VCCSM
AM27	VCCSM
AM28	VSS
AM29	VCCSM
AM30	SCLK_A0#
AM31	VSS
AM32	VCCSM
AM33	SCS_B1#
AM34	SMA_B13
AM35	----
AN1	VSS
AN2	SCLK_A1
AN3	SCLK_A1#
AN4	SDQ_A10
AN5	SDQ_A21
AN6	SDQ_B15
AN7	SDQS_A2#
AN8	SCKE_B3

Ball	DDR2 Signal Name
AN9	SBS_B2
AN10	SMA_B12
AN11	SMA_B5
AN12	----
AN13	SMA_B4
AN14	SMA_B2
AN15	SMA_B0
AN16	SBS_B1
AN17	SRAS_B#
AN18	SCKE_A2
AN19	SCKE_A1
AN20	SMA_A12
AN21	SMA_A7
AN22	SMA_A5
AN23	SMA_A8
AN24	----
AN25	SMA_A2
AN26	SMA_A0
AN27	SBS_A0
AN28	SWE_A#
AN29	SODT_A2
AN30	SMA_A13
AN31	SCS_A1#
AN32	SODT_A3
AN33	SCS_B2#
AN34	SODT_B0
AN35	VCCSM
AP1	NC
AP2	SDQ_A14
AP3	SDQ_A15
AP4	SDQ_A11
AP5	SDQ_A16
AP6	SDM_A2
AP7	SDQS_A2
AP8	VCCSM
AP9	SCKE_B1
AP10	SMA_B11
AP11	SMA_B9
AP12	VCCSM

Table 13-2. Intel® E7221 MCH DDR2 Signal List by Ball (Sheet 11 of 11)

Ball	DDR2 Signal Name
AP13	SMA_B6
AP14	SMA_B3
AP15	SMA_B10
AP16	VCCSM
AP17	SWE_B#
AP18	SCAS_B#
AP19	SCKE_A0
AP20	VCCSM
AP21	SMA_A11
AP22	SMA_A9
AP23	SMA_A4
AP24	VCCSM
AP25	SMA_A1
AP26	SMA_A10
AP27	SRAS_A#
AP28	VCCSM
AP29	SCAS_A#
AP30	SODT_A0
AP31	SCS_A3#
AP32	SODT_A1

Ball	DDR2 Signal Name
AP33	SCS_B0#
AP34	SCS_B3#
AP35	NC
AR1	NC
AR2	NC
AR3	VSS
AR4	----
AR5	SDQ_A20
AR6	VSS
AR7	VCCSM
AR8	SCKE_B2
AR9	SCKE_B0
AR10	VCCSM
AR11	SMA_B7
AR12	SMA_B8
AR13	VSS
AR14	VCCSM
AR15	SMA_B1
AR16	SBS_B0

Ball	DDR2 Signal Name
AR17	VSS
AR18	VCCSM
AR19	SCKE_A3
AR20	SBS_A2
AR21	VSS
AR22	VCCSM
AR23	SMA_A6
AR24	SMA_A3
AR25	VSS
AR26	VCCSM
AR27	SBS_A1
AR28	SCS_A2#
AR29	SCS_A0#
AR30	VSS
AR31	VCCSM
AR32	----
AR33	VCCSM
AR34	NC
AR35	NC

13.3 DDR Ballmap

Figure 13-3 and Figure 13-4 diagram the MCH ballout for platforms using a DDR system memory as viewed from the top side of the package. They are broken into a left side view and a right side view. Following the ballmap diagrams are two signal lists; the first is sorted by name and the second is sorted by ball location.

Figure 13-3. Intel® E7221 MCH DDR Ballout – Top View, Left Side

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A		NC	VSS		VSS	EXP_TXN3	EXP_TXP3	EXP_TXN1	EXP_TXP1	VSS	GCLKP	VCCA_DPLLA	VCC2	VCCA_EXPPLL	CRTIREFSET	RSV	VCCA_HPLL	VSS
B	NC	VSS	EXP_RXP4	EXP_RXN4	VSS	VSS	VSS	VSS	VSS	VSS	GCLKN	VSS	VCCA_DPLLB	VSS	RSV	VSS	VCCA_SMPLL	VSS
C	VSS	EXP_TXP5	VSS	VSS	EXP_TXN4	EXP_TXP4	EXP_TXN2	EXP_TXP2	EXP_TXN0	EXP_TXP0	VSS		VSS	RSV	MTYPE	NC	VSS	VSS
D		EXP_TXN5	VSS	VSS	EXP_RXP5	VSS	VSS	VSS	VSS	VSS	VSS	CRTVSYNC	VCCA_DAC	CRTGREEN	VSS	VSS	BSEL2	VSS
E	VSS	VSS	EXP_TXP6	VSS	EXP_RXN5	VSS	EXP_RXN3	VSS	EXP_RXN2	VSS	EXP_RXP0	CRTHSYNC	VCCA_DAC	CRTGREEN#	BSEL1	NC	VSS	VSS
F	EXP_TXP7	VSS	EXP_TXN6	VSS	VSS	VSS	EXP_RXP3	VSS	EXP_RXP2	VSS	EXP_RXN0	NC	VSSA_DAC	CRTRED	RSV	VSS	HD47	VSS
G	EXP_TXN7	VSS	RSV	VSS	EXP_RXN6	EXP_RXP6	VSS	VSS	VSS	VSS	VSS	NC	VSS	CRTRED#	VSS	RSV	VSS	HD45
H	RSV	VSS	RSV	VSS	VSS	VSS	EXP_RXN7	EXP_RXP7	VSS	VSS	EXP_RXN1	NC	VSS	CRTBLUE	NC	BSEL0	NC	HD46
J	RSV	VSS	RSV	VSS	RSV	RSV	VSS	VSS	VSS	VSS	EXP_RXP1	NC	RSV	CRTBLUE#	VSS	VSS	VSS	VSS
K	RSV	VSS	RSV	VSS	VSS	VSS	RSV	RSV	VSS	VSS	VSS	NC	RSV	VSS	RSV	EXTTS#	HD44	HD43
L	RSV	VSS	RSV	VSS	RSV	RSV	VSS	VSS	VSS	VCC	VSS	NC	VSS	CRTDDCDATA	VSS	VSS	VSS	VSS
M	RSV	VSS	RSV	VSS	VSS	VSS	RSV	RSV	VSS	VSS	VSS	DREFCLKN	DREFCLKP	ICH_SYNC#	CRTDDCCLK	RSV	VSS	HD42
N	RSV	VSS	RSV	VSS	RSV	RSV	VSS	VSS	VSS	VSS	VSS	NC	VCC	VCC	VCC	VCC	VSS	VCC
P	RSV	VSS	RSV	VSS	VSS	VSS	RSV	RSV	VSS	RSV	VSS	NC	VCC	VCC	VCC	VSS	VCC	VSS
R	RSV	VSS	DMI_TXP0	VSS	RSV	RSV	VSS	VSS	VSS	RSV	VSS	NC	VCC	VCC	VCC	VCC	VSS	VCC
T	DMI_TXP1	VSS	DMI_TXN0	VSS	VSS	VSS	VSS	DMI_RXN1	DMI_RXP1	VSS	VSS	NC	VCC	VCC	VCC	VCC	VCC	VSS
U	DMI_TXN1	VSS	DMI_TXP2	VSS	DMI_RXP0	DMI_RXN0	VSS	VSS	VSS	DMI_RXN3	VSS	NC	VCC	VCC	VSS	VCC	VSS	VCC
V	VSS	VSS	DMI_TXN2	VSS	DMI_TXP3	VSS	DMI_RXP2	DMI_RXN2	VSS	DMI_RXP3	VSS	NC	VCC	VCC	VCC	VSS	VCC	VSS
W	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	DMI_TXN3	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_COMPI	VSS	NC	VCC	VCC	VSS	VCC	VSS	VCC
Y	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_COMPO	VSS	NC	VCC	VCC	VCC	VCC	VCC	VSS
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	VCC	VCC	VSS	VCC	VSS	VCC
AB	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	NC	VCC	VCC	VCC	VCC	VCC	VCC
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	RSV	RSV	RSV	RSV	RSV	RSV	RSV
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	SDQ_B20	VSS	SDQ_B17	SDQ_B29	VSS	SDQ_A29	SDQ_B24
AE	SDQ_A5	SDQ_A4	SDQ_A0	VSS	SOCOMP1	VSS	SVREF0	SVREF1	VSS	SMSLEWOUT1	SDQ_B4	VSS	SDQ_B21	SDQ_B19	SDQ_A28	RSV_TP0	SDQ_A24	NC
AF	VSS	SDM_A0	SDQ_A1	VSS	SOCOMP0	VSS	RSTIN#	VSS	SMSLEWIN1	VSS	SDQ_B5	SDQ_B11	SDQ_B16	SDQ_B18	SDQ_B28	SDQ_A25	SDM_A3	VSS
AG	SDQS_A0	SDQS_A0#	SDQ_A6	SRCOMP0	VSS	NC	PWROK	SRCOMP1	VSS	SDQ_B1	SDQ_B0	VSS	VSS	SDQS_B2#	VSS	VSS	SDQS_A3#	VSS
AH	VSS	SDQ_A7	SDQ_A2	SDQ_B12	NC	VSS	SDQ_B7	SDQS_B0	SDQS_B0#	SDM_B0	VSS	SDM_B2	SDQS_B2	VSS	RSV_TP1	SDQS_A3	SDQ_A27	VSS
AJ	SDQ_A12	SDQ_A3	SDQ_A13	VSS	SDQ_B13	SDQ_B3	SDQ_B2	SDQ_B6	VSS	VSS	SCLK_B4	SMSLEWIN0	VSS	NC	VSS	VSS	SDQ_A31	SCB_B1
AK	VSS	SDQ_A8	SDQ_A9	VSS	SDM_B1	VSS	SDQ_A17	VSS	SCLK_B1	SDQ_B8	VSS	SMSLEWOUT0	SDQ_B22	VSS	RSV_TP3	SDQ_A30	VSS	SCB_B5
AL	SDM_A1	SDQS_A1#	SDQS_A1	SDQ_B9	SDQS_B1#	SDQ_B14	SDQ_A19	SDQ_B10	SCLK_B1#	VSS	SCLK_B4#	VCCSM	VSS	SDQ_B23	RSV_TP2	VSS	SDQ_A26	SDQ_B26
AM		SCLK_A4#	SCLK_A4	VSS	SDQS_B1	VSS	SDQ_A22	SDQ_A23	SDQ_A18	VCCSM	VCCSM	NC	VCCSM	VCCSM	NC	VCCSM	VCCSM	NC
AN	VSS	SCLK_A1	SCLK_A1#	SDQ_A10	SDQ_A21	SDQ_B15	SDQS_A2#	SCKE_B3	SBS_B2	SMA_B12	SMA_B5		SMA_B4	SMA_B2	SMA_B0	SBS_B1	SRAS_B#	SCKE_A2
AP	NC	SDQ_A14	SDQ_A15	SDQ_A11	SDQ_A16	SDM_A2	SDQS_A2	VCCSM	SCKE_B1	SMA_B11	SMA_B9	VCCSM	SMA_B6	SMA_B3	SMA_B10	VCCSM	SWE_B#	SCAS_B#
AR	NC	NC	VSS		SDQ_A20	VSS	VCCSM	SCKE_B2	SCKE_B0	VCCSM	SMA_B7	SMA_B8	VSS	VCCSM	SMA_B1	SBS_B0	VSS	VCCSM
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

Figure 13-4. Intel® E7221 MCH DDR Ballout – Top View, Right Side

	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
A	VTT	VTT	VTT	VTT	HSWING	HVREF	HD48	VSS	HD61	HD57	HD55	VSS	HD53		VSS	NC	NC
B	VTT	VTT	VTT	VTT	HRCOMP	VSS	HD63	HDINV3#	HD54	VSS	HDSTBP3#	HD51	HD52	HD15	HD13	HD11	NC
C	VTT	VTT	VTT	VTT	VSS		HD58	HD59	HD49	HD56	HDSTBN3#	HD17	HD50	HD14	HD9	HD12	VSS
D	VTT	VTT	VTT	VTT	VSS	HSCOMP	VSS	VSS	HD60	VSS	HD18	VSS	VSS	VSS	HD10	HD8	
E	VTT	VTT	VTT	VTT	VSS	HD62	HD25	VSS	HD24	HD16	VSS	HBPRI#	HPCREQ#	HREQ1#	HDSTBP0#	HDINV0#	HDSTBN0#
F	HDSTBN2#	VTT	VTT	VTT	VSS	NC	VSS	HDSTBN1#	HD23	HD22	VSS	VSS	HREQ4#	VSS	HREQ0#	HD6	VSS
G	VSS	VSS	VTT	VTT	VSS	HCPURST#	HD26	VSS	VSS	VSS	HD20	HA6#	HREQ3#	HA7#	HD7	HD5	HD3
H	HD41	HD40	VSS	VTT	HD37	VSS	VSS	HDSTBP1#	VSS	HD19	HA3#	VSS	HREQ2#	VSS	HD1	VSS	HD4
J	HDSTBP2#	VSS	HD35	HD32	VSS	HD33	HD27	HDINV1#	HD21	HA13#	HA5#	VSS	HADSTB0#	HRS2#	HD0	HD2	HDEFER#
K	HDINV2#	VSS	HD39	HD34	HD31	VSS	HD28	VSS	HA14#	VSS	HA4#	HA8#	VSS	VSS	HA15#	HRS0#	VSS
L	NC	VSS	VSS	VSS	HD30	VSS	HD29	HA18#	VSS	HA12#	HA9#	VSS	HA11#	VSS	HLOCK#	HHIT#	HDBSY#
M	HD38	VSS	HD36	HCLKN	HCLKP	VSS	VSS	HA20#	VSS	HA16#	VSS	HA10#	HADS#	HDRDY#		VSS	HBNR#
N	VSS	VCC	VCC	NC	NC	NC	VSS	HA19#	HADSTB1#	VSS	HA23#	VSS	HA21#	VSS	HA26#	HTRDY#	HHITM#
P	VCC	VSS	VCC	VCC	NC	NC	VSS	HA22#	VSS	HA24#	VSS	NC	VSS	VSS	HEDRDY#	HRS1#	VSS
R	VSS	VCC	VSS	VCC	VCC	NC	VSS	VSS	VSS	HA25#	HA17#	SCB_A4	SCB_A5	SDQ_A58	HBREQ0#	SDQ_A59	RSV
T	VCC	VCC	VCC	VSS	VCC	VCC	VSS	HA30#	HA27#	VSS	HA31#	VSS	HA28#	VSS	SDQ_A62	VSS	SDQ_A63
U	VSS	VCC	VSS	VCC	VSS	VCC	VSS	SDQ_B63	VSS	HA29#	VSS	SDQS_A8#	VSS	VSS	SDM_A7	SDQS_A7	SDQS_A7#
V	VCC	VSS	VCC	VSS	VCC	VCC	VSS	VSS	VSS	SDQ_B58	SDQ_B59	SDQS_A8	SCB_A1	SCB_A0	SDQ_A57	SDQ_A56	VSS
W	VSS	VCC	VSS	VCC	VSS	VCC	VSS	SDQ_B62	SDQS_B7	VSS	SDQ_B57	VSS	SDM_B7	VSS	SDQ_A61	SDQ_A51	SDQ_A60
Y	VCC	VCC	VCC	VSS	VCC	VCC	VSS	SDQ_B60	VSS	SDQS_B7#	VSS	SCB_A6	VSS	VSS	SDQ_A50	VSS	SDQ_A55
AA	VSS	VCC	VCC	VCC	VCC	VCC	VSS	VSS	VSS	SDQ_B56	SDQ_B61	SCB_A3	SCB_A2	SDQ_A54	SDM_A6	SDQS_A6	SDQS_A6#
AB	VCC	VCC	VCC	VCC	VCC	VCC	VSS	SDQ_B51	SDQ_B55	VSS	SCB_A7	VSS	SDQS_B6	VSS	RSV	SCLK_A5#	VSS
AC	RSV	RSV	RSV	RSV	NC	NC	VSS	SDQ_B50	VSS	SDQ_B54	VSS	SDQS_B6#	VSS	VSS	SCLK_A5	SCLK_A2	SCLK_A2#
AD	VSS	VSS	NC	VSS	SDQ_B37	SDM_B6	VSS	VSS	SDQ_A35	SCLK_B5	SCLK_B5#	NC	SDQ_A48	RSV		VSS	SDQ_A49
AE	SDQ_B25	SDM_B3	VSS	VSS	VSS	VSS	SCLK_B2#	SCLK_B2	SDQ_B49	VSS	SDQ_B53	NC	SDQ_B52	VSS	SDQ_A43	SDQ_A53	SDQ_A52
AF	NC	SDQS_B3#	VSS	NC	SDQ_B36	SDQ_B32	SDM_B4	VSS	SDQ_B48	SDQ_A39	VSS	SDQ_B43	VSS	VSS	SDQ_A42	SDQ_A47	VSS
AG	VSS	SDQS_B3	VSS	VSS	SCLK_B0#	SDQ_B33	NC	SDQS_B4#	SDQ_A38	SDQ_B47	NC	SDQ_B46	SDQ_B42	SDQ_A46	SDQS_A5#	SDM_A5	SDQS_A5
AH	SDQ_B30	VSS	SDQ_B31	VSS	SCLK_B0	NC	SDQS_B4	VSS	SDQ_A34	SDQS_B5	VSS	SDQS_B5#	SDM_B5	VSS	VSS	SDQ_A40	SDQ_A41
AJ	VSS	SCB_B0	SDQS_B8#	VSS	SCB_B2	SCB_B3	SDQ_B39	SDQ_B35	VSS	SDQS_A4#	SDQ_B44	VSS	SDQ_B41	VSS	SDM_A4	SDQ_A45	VSS
AK	SDQ_B27	VSS	SDQS_B8	SCLK_B3#	VSS	NC	VSS	VSS	SDQS_A4	SCLK_A3#	SDQ_A32	VSS	SDQ_A33	SDQ_B40	SDQ_B45	SDQ_A44	VCCSM
AL	VSS	SCB_B4	SCB_B6	SCB_B7	SCLK_B3	VSS	SDQ_B38	SDQ_B34	NC	SCLK_A3	SCLK_A0	SDQ_A36	SDQ_A37	VSS	SODT_B3	SODT_B1	SODT_B2
AM	VCCSM	VCCSM	NC	VCCSM	VCCSM	NC	VCCSM	VCCSM	VCCSM	VSS	VCCSM	SCLK_A0#	VSS	VCCSM	SCS_B1#	SMA_B13	
AN	SCKE_A1	SMA_A12	SMA_A7	SMA_A5	SMA_A8		SMA_A2	SMA_A0	SBS_A0	SWE_A#	SODT_A2	SMA_A13	SCS_A1#	SODT_A3	SCS_B2#	SODT_B0	VCCSM
AP	SCKE_A0	VCCSM	SMA_A11	SMA_A9	SMA_A4	VCCSM	SMA_A1	SMA_A10	SRAS_A#	VCCSM	SCAS_A#	SODT_A0	SCS_A3#	SODT_A1	SCS_B0#	SCS_B3#	NC
AR	SCKE_A3	SBS_A2	VSS	VCCSM	SMA_A6	SMA_A3	VSS	VCCSM	SBS_A1	SCS_A2#	SCS_A0#	VSS	VCCSM		VCCSM	NC	NC

13.4 MCH DDR Ballout Signal Lists

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 1 of 11)

Signal Name DDR	Ball
BSEL0	H16
BSEL1	E15
BSEL2	D17
CRTBLUE	H14
CRTBLUE#	J14
CRTDDCCLK	M15
CRTDDCDATA	L14
CRTGREEN	D14
CRTGREEN#	E14
CRTHSYNC	E12
CRTIREFSET	A15
CRTRED	F14
CRTRED#	G14
CRTVSYNC	D12
DMI_RXN0	U6
DMI_RXN1	T8
DMI_RXN2	V8
DMI_RXN3	U10
DMI_RXP0	U5
DMI_RXP1	T9
DMI_RXP2	V7
DMI_RXP3	V10
DMI_TXN0	T3
DMI_TXN1	U1
DMI_TXN2	V3
DMI_TXN3	W5
DMI_TXP0	R3
DMI_TXP1	T1
DMI_TXP2	U3
DMI_TXP3	V5
DREFCLKN	M12
DREFCLKP	M13
EXP_COMPI	W10
EXP_COMPO	Y10
EXP_RXN0	F11
EXP_RXN1	H11
EXP_RXN2	E9
EXP_RXN3	E7
EXP_RXN4	B4
EXP_RXN5	E5
EXP_RXN6	G5
EXP_RXN7	H7
EXP_RXP0	E11
EXP_RXP1	J11
EXP_RXP2	F9
EXP_RXP3	F7
EXP_RXP4	B3
EXP_RXP5	D5
EXP_RXP6	G6
EXP_RXP7	H8
EXP_TXN0	C9
EXP_TXN1	A8
EXP_TXN2	C7
EXP_TXN3	A6
EXP_TXN4	C5
EXP_TXN5	D2
EXP_TXN6	F3
EXP_TXN7	G1
EXP_TXP0	C10
EXP_TXP1	A9
EXP_TXP2	C8
EXP_TXP3	A7
EXP_TXP4	C6
EXP_TXP5	C2
EXP_TXP6	E3
EXP_TXP7	F1
EXTTS#	K16
GCLKN	B11
GCLKP	A11
HA10#	M30
HA11#	L31
HA12#	L28
HA13#	J28
HA14#	K27
HA15#	K33
HA16#	M28
HA17#	R29
HA18#	L26
HA19#	N26
HA20#	M26
HA21#	N31
HA22#	P26
HA23#	N29
HA24#	P28
HA25#	R28
HA26#	N33
HA27#	T27
HA28#	T31
HA29#	U28
HA3#	H29
HA30#	T26
HA31#	T29
HA4#	K29
HA5#	J29
HA6#	G30
HA7#	G32
HA8#	K30
HA9#	L29
HADS#	M31
HADSTB0#	J31
HADSTB1#	N27
HBNR#	M35
HBPRI#	E30
HBREQ0#	R33
HCLKN	M22
HCLKP	M23
HCPURST#	G24
HD0	J33
HD1	H33
HD10	D33
HD11	B34
HD12	C34
HD13	B33
HD14	C32

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 2 of 11)

Signal Name DDR	Ball
HD15	B32
HD16	E28
HD17	C30
HD18	D29
HD19	H28
HD2	J34
HD20	G29
HD21	J27
HD22	F28
HD23	F27
HD24	E27
HD25	E25
HD26	G25
HD27	J25
HD28	K25
HD29	L25
HD3	G35
HD30	L23
HD31	K23
HD32	J22
HD33	J24
HD34	K22
HD35	J21
HD36	M21
HD37	H23
HD38	M19
HD39	K21
HD4	H35
HD40	H20
HD41	H19
HD42	M18
HD43	K18
HD44	K17
HD45	G18
HD46	H18
HD47	F17
HD48	A25
HD49	C27
HD5	G34
NC	AM24

Signal Name DDR	Ball
HD50	C31
HD51	B30
HD52	B31
HD53	A31
HD54	B27
HD55	A29
HD56	C28
HD57	A28
HD58	C25
HD59	C26
HD6	F34
HD60	D27
HD61	A27
HD62	E24
HD63	B25
HD7	G33
HD8	D34
HD9	C33
HDBSY#	L35
HDEFER#	J35
HDINV0#	E34
HDINV1#	J26
HDINV2#	K19
HDINV3#	B26
HDRDY#	M32
HDSTBN0#	E35
HDSTBN1#	F26
HDSTBN2#	F19
HDSTBN3#	C29
HDSTBP0#	E33
HDSTBP1#	H26
HDSTBP2#	J19
HDSTBP3#	B29
HEDRDY#	P33
HHIT#	L34
HHITM#	N35
HLOCK#	L33
HPCREQ#	E31
HRCOMP	B23
NC	R12

Signal Name DDR	Ball
HREQ0#	F33
HREQ1#	E32
HREQ2#	H31
HREQ3#	G31
HREQ4#	F31
HRS0#	K34
HRS1#	P34
HRS2#	J32
HSCOMP	D24
HSWING	A23
HTRDY#	N34
HVREF	A24
ICH_SYNC#	M14
MTYPE	C15
NC	A2
NC	A34
NC	A35
NC	AA12
NC	AB12
NC	AC23
NC	AC24
NC	AD21
NC	AD30
NC	AE18
NC	AE30
NC	AF19
NC	AF22
NC	AG25
NC	AG29
NC	AG6
NC	AH24
NC	AH5
NC	AJ14
NC	AK24
NC	AL27
NC	AM12
NC	AM15
NC	AM18
NC	AM21
RSV	G3

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 3 of 11)

Signal Name DDR	Ball
NC	AN25
NC	AN29
NC	AN31
NC	AN32
NC	AP1
NC	AP25
NC	AP30
NC	AP31
NC	AP32
NC	AP35
NC	AR1
NC	AR2
NC	AR28
NC	AR29
NC	AR34
NC	AR35
NC	B1
NC	B35
NC	C16
NC	E16
NC	F12
NC	F24
NC	G12
NC	H12
NC	H15
NC	H17
NC	J12
NC	K12
NC	L12
NC	L19
NC	N12
NC	N22
NC	N23
NC	N24
NC	P12
NC	P23
NC	P24
NC	P30
RSV (SDQS_B5#)	AH30
RSV (SDQS_B6#)	AC30

Signal Name DDR	Ball
NC	R24
NC	T12
NC	U12
NC	V12
NC	W12
NC	Y12
PWROK	AG7
RSTIN#	AF7
RSV	L5
RSV	R10
RSV	M7
RSV	N5
RSV	P8
RSV	R5
RSV	J5
RSV	K7
RSV	L6
RSV	P10
RSV	M8
RSV	N6
RSV	P7
RSV	R6
RSV	J6
RSV	K8
RSV	K3
RSV	L1
RSV	M3
RSV	N1
RSV	P3
RSV	R1
RSV	H3
RSV	J1
RSV	J3
RSV	K1
RSV	L3
RSV	M1
RSV	N3
RSV	P1
SCKE_B3	AR8
SCLK_A0	AK28

Signal Name DDR	Ball
RSV	H1
RSV	A16
RSV	AC12
RSV	AC13
RSV	AC14
RSV	AC15
RSV	AC16
RSV	AC17
RSV	AC18
RSV	AC19
RSV	AC20
RSV	AC21
RSV	AC22
RSV	B15
RSV	C14
RSV	F15
RSV	G16
RSV	J13
RSV	K13
RSV	K15
RSV	M16
RSV	R35
RSV (SBS_A2)	AP23
RSV (SBS_B2)	AR24
RSV (SDQS_A0#)	AG2
RSV (SDQS_A1#)	AL2
RSV (SDQS_A2#)	AN7
RSV (SDQS_A3#)	AG17
RSV (SDQS_A4#)	AJ28
RSV (SDQS_A5#)	AG33
RSV (SDQS_A6#)	AA35
RSV (SDQS_A7#)	U35
RSV (SDQS_A8#)	U30
RSV (SDQS_B0#)	AH9
RSV (SDQS_B1#)	AL5
RSV (SDQS_B2#)	AG14
RSV (SDQS_B3#)	AF20
RSV (SDQS_B4#)	AG26
SDM_A6	AA33
SDM_A7	U33

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 4 of 11)

Signal Name DDR	Ball
RSV (SDQS_B7#)	Y28
RSV (SDQS_B8#)	AJ21
RSV (SOCOMP0)	AF5
RSV (SOCOMP1)	AE5
RSV_TP0	AE16
RSV_TP1	AH15
RSV_TP2	AL15
RSV_TP3	AK15
SBS_A0	AN28
SBS_A1	AN26
SBS_B0	AP26
SBS_B1	AR19
SCAS_A#	AL34
SCAS_B#	AR27
SCB_A0	V32
SCB_A1	V31
SCB_A2	AA31
SCB_A3	AA30
SCB_A4	R30
SCB_A5	R31
SCB_A6	Y30
SCB_A7	AB29
SCB_B0	AJ20
SCB_B1	AJ18
SCB_B2	AJ23
SCB_B3	AJ24
SCB_B4	AL20
SCB_B5	AK18
SCB_B6	AL21
SCB_B7	AL22
SCKE_A0	AR11
SCKE_A1	AN9
SCKE_A2	AP10
SCKE_A3	AN10
SCKE_B0	AP9
SCKE_B1	AN8
SCKE_B2	AR9
SDQ_A35	AD27
SDQ_A36	AL30
SDQ_A37	AL31

Signal Name DDR	Ball
SCLK_A0#	AL28
SCLK_A1	AM2
SCLK_A1#	AM3
SCLK_A2	AB34
SCLK_A2#	AC33
SCLK_A3	AM30
SCLK_A3#	AL29
SCLK_A4	AN2
SCLK_A4#	AN3
SCLK_A5	AC35
SCLK_A5#	AC34
SCLK_B0	AH23
SCLK_B0#	AG23
SCLK_B1	AL11
SCLK_B1#	AJ11
SCLK_B2	AE26
SCLK_B2#	AE25
SCLK_B3	AL23
SCLK_B3#	AK22
SCLK_B4	AK9
SCLK_B4#	AL9
SCLK_B5	AD29
SCLK_B5#	AD28
SCS_A0#	AM33
SCS_A1#	AL35
SCS_A2#	AL33
SCS_A3#	AM34
SCS_B0#	AN33
SCS_B1#	AP34
SCS_B2#	AP33
SCS_B3#	AN34
SDM_A0	AF2
SDM_A1	AL1
SDM_A2	AP6
SDM_A3	AF17
SDM_A4	AJ33
SDM_A5	AG34
SDQ_B12	AH4
SDQ_B13	AJ5
SDQ_B14	AL6

Signal Name DDR	Ball
SDM_B0	AH10
SDM_B1	AK5
SDM_B2	AH12
SDM_B3	AE20
SDM_B4	AF25
SDM_B5	AH31
SDM_B6	AD24
SDM_B7	W31
SDQ_A0	AE3
SDQ_A1	AF3
SDQ_A10	AN4
SDQ_A11	AP4
SDQ_A12	AJ1
SDQ_A13	AJ3
SDQ_A14	AP2
SDQ_A15	AP3
SDQ_A16	AP5
SDQ_A17	AK7
SDQ_A18	AM9
SDQ_A19	AL7
SDQ_A2	AH3
SDQ_A20	AR5
SDQ_A21	AN5
SDQ_A22	AM7
SDQ_A23	AM8
SDQ_A24	AE17
SDQ_A25	AF16
SDQ_A26	AL17
SDQ_A27	AH17
SDQ_A28	AE15
SDQ_A29	AD17
SDQ_A3	AJ2
SDQ_A30	AK16
SDQ_A31	AJ17
SDQ_A32	AK29
SDQ_A33	AK31
SDQ_A34	AH27
SDQ_B48	AF27
SDQ_B49	AE27
SDQ_B5	AF11

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 5 of 11)

Signal Name DDR	Ball
SDQ_A38	AG27
SDQ_A39	AF28
SDQ_A4	AE2
SDQ_A40	AH34
SDQ_A41	AH35
SDQ_A42	AF33
SDQ_A43	AE33
SDQ_A44	AK34
SDQ_A45	AJ34
SDQ_A46	AG32
SDQ_A47	AF34
SDQ_A48	AD31
SDQ_A49	AD35
SDQ_A5	AE1
SDQ_A50	Y33
SDQ_A51	W34
SDQ_A52	AE35
SDQ_A53	AE34
SDQ_A54	AA32
SDQ_A55	Y35
SDQ_A56	V34
SDQ_A57	V33
SDQ_A58	R32
SDQ_A59	R34
SDQ_A6	AG3
SDQ_A60	W35
SDQ_A61	W33
SDQ_A62	T33
SDQ_A63	T35
SDQ_A7	AH2
SDQ_A8	AK2
SDQ_A9	AK3
SDQ_B0	AG11
SDQ_B1	AG10
SDQ_B10	AL8
SDQ_B11	AF12
SMA_A0	AN23
SMA_A1	AN22
SMA_A10	AR23
SMA_A11	AP15

Signal Name DDR	Ball
SDQ_B15	AN6
SDQ_B16	AF13
SDQ_B17	AD14
SDQ_B18	AF14
SDQ_B19	AE14
SDQ_B2	AJ7
SDQ_B20	AD12
SDQ_B21	AE13
SDQ_B22	AK13
SDQ_B23	AL14
SDQ_B24	AD18
SDQ_B25	AE19
SDQ_B26	AL18
SDQ_B27	AK19
SDQ_B28	AF15
SDQ_B29	AD15
SDQ_B3	AJ6
SDQ_B30	AH19
SDQ_B31	AH21
SDQ_B32	AF24
SDQ_B33	AG24
SDQ_B34	AL26
SDQ_B35	AJ26
SDQ_B36	AF23
SDQ_B37	AD23
SDQ_B38	AL25
SDQ_B39	AJ25
SDQ_B4	AE11
SDQ_B40	AK32
SDQ_B41	AJ31
SDQ_B42	AG31
SDQ_B43	AF30
SDQ_B44	AJ29
SDQ_B45	AK33
SDQ_B46	AG30
SDQ_B47	AG28
SWE_B#	AN27
VCC	AA13
VCC	AA14
VCC	AA16

Signal Name DDR	Ball
SDQ_B50	AC26
SDQ_B51	AB26
SDQ_B52	AE31
SDQ_B53	AE29
SDQ_B54	AC28
SDQ_B55	AB27
SDQ_B56	AA28
SDQ_B57	W29
SDQ_B58	V28
SDQ_B59	V29
SDQ_B6	AJ8
SDQ_B60	Y26
SDQ_B61	AA29
SDQ_B62	W26
SDQ_B63	U26
SDQ_B7	AH7
SDQ_B8	AK10
SDQ_B9	AL4
SDQS_A0	AG1
SDQS_A1	AL3
SDQS_A2	AP7
SDQS_A3	AH16
SDQS_A4	AK27
SDQS_A5	AG35
SDQS_A6	AA34
SDQS_A7	U34
SDQS_A8	V30
SDQS_B0	AH8
SDQS_B1	AM5
SDQS_B2	AH13
SDQS_B3	AG20
SDQS_B4	AH25
SDQS_B5	AH28
SDQS_B6	AB31
SDQS_B7	W27
SDQS_B8	AK21
VCC	AC5
VCC	AC6
VCC	AC7
VCC	AC8

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 6 of 11)

Signal Name DDR	Ball
SMA_A12	AP13
SMA_A13	AB33
SMA_A2	AP22
SMA_A3	AN21
SMA_A4	AP21
SMA_A5	AP19
SMA_A6	AN20
SMA_A7	AN16
SMA_A8	AN18
SMA_A9	AN15
SMA_B0	AN19
SMA_B1	AP18
SMA_B10	AR20
SMA_B11	AP11
SMA_B12	AN11
SMA_B13	AD32
SMA_B2	AN17
SMA_B3	AR16
SMA_B4	AR15
SMA_B5	AN14
SMA_B6	AP17
SMA_B7	AP14
SMA_B8	AN13
SMA_B9	AR12
SM_SLEWIN0	AJ12
SM_SLEWIN1	AF9
SM_SLEWOUT0	AK12
SM_SLEWOUT1	AE10
SRAS_A#	AP29
SRAS_B#	AP27
SRCOMP0	AG4
SRCOMP1	AG8
SVREF0	AE7
SVREF1	AE8
SWE_A#	AN30
VCC	T14
VCC	T15
VCC	T16
VCC	T17
VCC	T19
VCC	AA18
VCC	AA20
VCC	AA21
VCC	AA22
VCC	AA23
VCC	AA24
VCC	AB1
VCC	AB10
VCC	AB11
VCC	AB13
VCC	AB14
VCC	AB15
VCC	AB16
VCC	AB17
VCC	AB18
VCC	AB19
VCC	AB2
VCC	AB20
VCC	AB21
VCC	AB22
VCC	AB23
VCC	AB24
VCC	AB3
VCC	AB4
VCC	AB5
VCC	AB6
VCC	AB7
VCC	AB8
VCC	AB9
VCC	AC1
VCC	AC10
VCC	AC11
VCC	AC2
VCC	AC3
VCC	AC4
VCC	Y23
VCC	Y24
VCC_EXP	W1
VCC_EXP	W2
VCC_EXP	W3
VCC	AC9
VCC	AD1
VCC	AD10
VCC	AD2
VCC	AD3
VCC	AD4
VCC	AD5
VCC	AD6
VCC	AD7
VCC	AD8
VCC	AD9
VCC	L10
VCC	N13
VCC	N14
VCC	N15
VCC	N16
VCC	N18
VCC	N20
VCC	N21
VCC	P13
VCC	P14
VCC	P15
VCC	P17
VCC	P19
VCC	P21
VCC	P22
VCC	R13
VCC	R14
VCC	R15
VCC	R16
VCC	R18
VCC	R20
VCC	R22
VCC	R23
VCC	T13
VCCSM	AM25
VCCSM	AM26
VCCSM	AM27
VCCSM	AM29
VCCSM	AM32

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 7 of 11)

Signal Name DDR	Ball
VCC	T20
VCC	T21
VCC	T23
VCC	T24
VCC	U13
VCC	U14
VCC	U16
VCC	U18
VCC	U20
VCC	U22
VCC	U24
VCC	V13
VCC	V14
VCC	V15
VCC	V17
VCC	V19
VCC	V21
VCC	V23
VCC	V24
VCC	W13
VCC	W14
VCC	W16
VCC	W18
VCC	W20
VCC	W22
VCC	W24
VCC	Y13
VCC	Y14
VCC	Y15
VCC	Y16
VCC	Y17
VCC	Y19
VCC	Y20
VCC	Y21
VSS	AA5
VSS	AA6
VSS	AA7
VSS	AA8
VSS	AA9
VSS	AB25

Signal Name DDR	Ball
VCC_EXP	W4
VCC_EXP	W6
VCC_EXP	W7
VCC_EXP	W8
VCC_EXP	W9
VCC_EXP	Y1
VCC_EXP	Y2
VCC_EXP	Y3
VCC_EXP	Y4
VCC_EXP	Y5
VCC_EXP	Y6
VCC_EXP	Y7
VCC_EXP	Y8
VCC_EXP	Y9
VCC2	A13
VCCA_DAC	D13
VCCA_DAC	E13
VCCA_DPLLA	A12
VCCA_DPLLB	B13
VCCA_EXPPLL	A14
VCCA_HPLL	A17
VCCA_SMPLL	B17
VCCSM	AK35
VCCSM	AL12
VCCSM	AM10
VCCSM	AM11
VCCSM	AM13
VCCSM	AM14
VCCSM	AM16
VCCSM	AM17
VCCSM	AM19
VCCSM	AM20
VCCSM	AM22
VCCSM	AM23
VSS	AF29
VSS	AF31
VSS	AF32
VSS	AF35
VSS	AF4
VSS	AF6

Signal Name DDR	Ball
VCCSM	AN35
VCCSM	AP12
VCCSM	AP16
VCCSM	AP20
VCCSM	AP24
VCCSM	AP28
VCCSM	AP8
VCCSM	AR10
VCCSM	AR14
VCCSM	AR18
VCCSM	AR22
VCCSM	AR26
VCCSM	AR31
VCCSM	AR33
VCCSM	AR7
VSS	A10
VSS	A18
VSS	A26
VSS	A3
VSS	A30
VSS	A33
VSS	A5
VSS	AA1
VSS	AA10
VSS	AA11
VSS	AA15
VSS	AA17
VSS	AA19
VSS	AA2
VSS	AA25
VSS	AA26
VSS	AA27
VSS	AA3
VSS	AA4
VSS	AJ9
VSS	AK1
VSS	AK11
VSS	AK14
VSS	AK17
VSS	AK20

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 8 of 11)

Signal Name DDR	Ball
VSS	AB28
VSS	AB30
VSS	AB32
VSS	AB35
VSS	AC25
VSS	AC27
VSS	AC29
VSS	AC31
VSS	AC32
VSS	AD11
VSS	AD13
VSS	AD16
VSS	AD19
VSS	AD20
VSS	AD22
VSS	AD25
VSS	AD26
VSS	AD34
VSS	AE12
VSS	AE21
VSS	AE22
VSS	AE23
VSS	AE24
VSS	AE28
VSS	AE32
VSS	AE4
VSS	AE6
VSS	AE9
VSS	AF1
VSS	AF10
VSS	AF18
VSS	AF21
VSS	AF26
VSS	B5
VSS	B6
VSS	B7
VSS	B8
VSS	B9
VSS	C1
VSS	C11

Signal Name DDR	Ball
VSS	AF8
VSS	AG12
VSS	AG13
VSS	AG15
VSS	AG16
VSS	AG18
VSS	AG19
VSS	AG21
VSS	AG22
VSS	AG5
VSS	AG9
VSS	AH1
VSS	AH11
VSS	AH14
VSS	AH18
VSS	AH20
VSS	AH22
VSS	AH26
VSS	AH29
VSS	AH32
VSS	AH33
VSS	AH6
VSS	AJ10
VSS	AJ13
VSS	AJ15
VSS	AJ16
VSS	AJ19
VSS	AJ22
VSS	AJ27
VSS	AJ30
VSS	AJ32
VSS	AJ35
VSS	AJ4
VSS	E29
VSS	E4
VSS	E6
VSS	E8
VSS	F10
VSS	F16
VSS	F18

Signal Name DDR	Ball
VSS	AK23
VSS	AK25
VSS	AK26
VSS	AK30
VSS	AK4
VSS	AK6
VSS	AK8
VSS	AL10
VSS	AL13
VSS	AL16
VSS	AL19
VSS	AL24
VSS	AL32
VSS	AM28
VSS	AM31
VSS	AM4
VSS	AM6
VSS	AN1
VSS	AR13
VSS	AR17
VSS	AR21
VSS	AR25
VSS	AR3
VSS	AR30
VSS	AR6
VSS	B10
VSS	B12
VSS	B14
VSS	B16
VSS	B18
VSS	B2
VSS	B24
VSS	B28
VSS	H25
VSS	H27
VSS	H30
VSS	H32
VSS	H34
VSS	H4
VSS	H5

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 9 of 11)

Signal Name DDR	Ball
VSS	C13
VSS	C17
VSS	C18
VSS	C23
VSS	C3
VSS	C35
VSS	C4
VSS	D10
VSS	D11
VSS	D15
VSS	D16
VSS	D18
VSS	D23
VSS	D25
VSS	D26
VSS	D28
VSS	D3
VSS	D30
VSS	D31
VSS	D32
VSS	D4
VSS	D6
VSS	D7
VSS	D8
VSS	D9
VSS	E1
VSS	E10
VSS	E17
VSS	E18
VSS	E2
VSS	E23
VSS	E26
VSS	L15
VSS	L16
VSS	L17
VSS	L18
VSS	L2
VSS	L20
VSS	L21
VSS	L22

Signal Name DDR	Ball
VSS	F2
VSS	F23
VSS	F25
VSS	F29
VSS	F30
VSS	F32
VSS	F35
VSS	F4
VSS	F5
VSS	F6
VSS	F8
VSS	G10
VSS	G11
VSS	G13
VSS	G15
VSS	G17
VSS	G19
VSS	G2
VSS	G20
VSS	G23
VSS	G26
VSS	G27
VSS	G28
VSS	G4
VSS	G7
VSS	G8
VSS	G9
VSS	H10
VSS	H13
VSS	H2
VSS	H21
VSS	H24
VSS	N4
VSS	N7
VSS	N8
VSS	N9
VSS	P11
VSS	P16
VSS	P18
VSS	P2

Signal Name DDR	Ball
VSS	H6
VSS	H9
VSS	J10
VSS	J15
VSS	J16
VSS	J17
VSS	J18
VSS	J2
VSS	J20
VSS	J23
VSS	J30
VSS	J4
VSS	J7
VSS	J8
VSS	J9
VSS	K10
VSS	K11
VSS	K14
VSS	K2
VSS	K20
VSS	K24
VSS	K26
VSS	K28
VSS	K31
VSS	K32
VSS	K35
VSS	K4
VSS	K5
VSS	K6
VSS	K9
VSS	L11
VSS	L13
VSS	T32
VSS	T34
VSS	T4
VSS	T5
VSS	T6
VSS	T7
VSS	U11
VSS	U15

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 10 of 11)

Signal Name DDR	Ball
VSS	L24
VSS	L27
VSS	L30
VSS	L32
VSS	L4
VSS	L7
VSS	L8
VSS	L9
VSS	M10
VSS	M11
VSS	M17
VSS	M2
VSS	M20
VSS	M24
VSS	M25
VSS	M27
VSS	M29
VSS	M34
VSS	M4
VSS	M5
VSS	M6
VSS	M9
VSS	N10
VSS	N11
VSS	N17
VSS	N19
VSS	N2
VSS	N25
VSS	N28
VSS	N30
VSS	N32
VSS	W19
VSS	W21
VSS	W23
VSS	W25
VSS	W28
VSS	W30
VSS	W32
VSS	Y11
VSS	Y18

Signal Name DDR	Ball
VSS	P20
VSS	P25
VSS	P27
VSS	P29
VSS	P31
VSS	P32
VSS	P35
VSS	P4
VSS	P5
VSS	P6
VSS	P9
VSS	R11
VSS	R17
VSS	R19
VSS	R2
VSS	R21
VSS	R25
VSS	R26
VSS	R27
VSS	R4
VSS	R7
VSS	R8
VSS	R9
VSS	T10
VSS	T11
VSS	T18
VSS	T2
VSS	T22
VSS	T25
VSS	T28
VSS	T30
VSS	Y22
VSS	Y25
VSS	Y27
VSS	Y29
VSS	Y31
VSS	Y32
VSS	Y34
VSS	F13
VTT	A19

Signal Name DDR	Ball
VSS	U17
VSS	U19
VSS	U2
VSS	U21
VSS	U23
VSS	U25
VSS	U27
VSS	U29
VSS	U31
VSS	U32
VSS	U4
VSS	U7
VSS	U8
VSS	U9
VSS	V1
VSS	V11
VSS	V16
VSS	V18
VSS	V2
VSS	V20
VSS	V22
VSS	V25
VSS	V26
VSS	V27
VSS	V35
VSS	V4
VSS	V6
VSS	V9
VSS	W11
VSS	W15
VSS	W17
VTT	A20
VTT	A21
VTT	A22
VTT	B19
VTT	B20
VTT	B21
VTT	B22
VTT	C19
VTT	C20

Table 13-3. Intel® E7221 MCH DDR Signal List by Name (Sheet 11 of 11)

Signal Name DDR	Ball
VTT	C21
VTT	C22
VTT	D19
VTT	D20
VTT	D21
VTT	D22

Signal Name DDR	Ball
VTT	E19
VTT	E20
VTT	E21
VTT	E22
VTT	F20

Signal Name DDR	Ball
VTT	F21
VTT	F22
VTT	G21
VTT	G22
VTT	H22

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 1 of 11)

Ball	Signal Name DDR
A1	–
A2	NC
A3	VSS
A4	–
A5	VSS
A6	EXP_TXN3
A7	EXP_TXP3
A8	EXP_TXN1
A9	EXP_TXP1
A10	VSS
A11	GCLKP
A12	VCCA_DPLLA
A13	VCC2
A14	VCCA_EXPPLL
A15	CRTIREFSET
A16	RSV
A17	VCCA_HPLL
A18	VSS
A19	VTT
A20	VTT
A21	VTT
A22	VTT
A23	HSWING
A24	HVREF
A25	HD48
A26	VSS
A27	HD61
A28	HD57

Ball	Signal Name DDR
B4	EXP_RXN4
B5	VSS
B6	VSS
B7	VSS
B8	VSS
B9	VSS
B10	VSS
B11	GCLKN
B12	VSS
B13	VCCA_DPLLB
B14	VSS
B15	RSV
B16	VSS
B17	VCCA_SMPLL
B18	VSS
B19	VTT
B20	VTT
B21	VTT
B22	VTT
B23	HRCOMP
B24	VSS
B25	HD63
B26	HDINV3#
B27	HD54
B28	VSS
B29	HDSTBP3#
B30	HD51
B31	HD52

Ball	Signal Name DDR
C7	EXP_TXN2
C8	EXP_TXP2
C9	EXP_TXN0
C10	EXP_TXP0
C11	VSS
C12	–
C13	VSS
C14	RSV
C15	MTYPE
C16	NC
C17	VSS
C18	VSS
C19	VTT
C20	VTT
C21	VTT
C22	VTT
C23	VSS
C24	–
C25	HD58
C26	HD59
C27	HD49
C28	HD56
C29	HDSTBN3#
C30	HD17
C31	HD50
C32	HD14
C33	HD9
C34	HD12

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 2 of 11)

Ball	Signal Name DDR
A29	HD55
A30	VSS
A31	HD53
A32	–
A33	VSS
A34	NC
A35	NC
B1	NC
B2	VSS
B3	EXP_RXP4
D10	VSS
D11	VSS
D12	CRTVSYNC
D13	VCCA_DAC
D14	CRTGREEN
D15	VSS
D16	VSS
D17	BSEL2
D18	VSS
D19	VTT
D20	VTT
D21	VTT
D22	VTT
D23	VSS
D24	HSCOMP
D25	VSS
D26	VSS
D27	HD60
D28	VSS
D29	HD18
D30	VSS
D31	VSS
D32	VSS
D33	HD10
D34	HD8
D35	–
E1	VSS
E2	VSS
E3	EXP_TXP6

Ball	Signal Name DDR
B32	HD15
B33	HD13
B34	HD11
B35	NC
C1	VSS
C2	EXP_TXP5
C3	VSS
C4	VSS
C5	EXP_TXN4
C6	EXP_TXP4
E14	CRTGREEN#
E15	BSEL1
E16	NC
E17	VSS
E18	VSS
E19	VTT
E20	VTT
E21	VTT
E22	VTT
E23	VSS
E24	HD62
E25	HD25
E26	VSS
E27	HD24
E28	HD16
E29	VSS
E30	HBPRI#
E31	HPCREQ#
E32	HREQ1#
E33	HDSTBP0#
E34	HDINV0#
E35	HDSTBN0#
F1	EXP_TXP7
F2	VSS
F3	EXP_TXN6
F4	VSS
F5	VSS
F6	VSS
F7	EXP_RXP3

Ball	Signal Name DDR
C35	VSS
D1	–
D2	EXP_TXN5
D3	VSS
D4	VSS
D5	EXP_RXP5
D6	VSS
D7	VSS
D8	VSS
D9	VSS
F18	VSS
F19	HDSTBN2#
F20	VTT
F21	VTT
F22	VTT
F23	VSS
F24	NC
F25	VSS
F26	HDSTBN1#
F27	HD23
F28	HD22
F29	VSS
F30	VSS
F31	HREQ4#
F32	VSS
F33	HREQ0#
F34	HD6
F35	VSS
G1	EXP_TXN7
G2	VSS
G3	RSV
G4	VSS
G5	EXP_RXN6
G6	EXP_RXP6
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	VSS

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 3 of 11)

Ball	Signal Name DDR
E4	VSS
E5	EXP_RXN5
E6	VSS
E7	EXP_RXN3
E8	VSS
E9	EXP_RXN2
E10	VSS
E11	EXP_RXP0
E12	CRTHSYNC
E13	VCCA_DAC
G22	VTT
G23	VSS
G24	HCPURST#
G25	HD26
G26	VSS
G27	VSS
G28	VSS
G29	HD20
G30	HA6#
G31	HREQ3#
G32	HA7#
G33	HD7
G34	HD5
G35	HD3
H1	RSV
H2	VSS
H3	RSV
H4	VSS
H5	VSS
H6	VSS
H7	EXP_RXN7
H8	EXP_RXP7
H9	VSS
H10	VSS
H11	EXP_RXN1
H12	NC
H13	VSS
H14	CRTBLUE
H15	NC

Ball	Signal Name DDR
F8	VSS
F9	EXP_RXP2
F10	VSS
F11	EXP_RXN0
F12	NC
F13	VSS
F14	CRTRED
F15	RSV
F16	VSS
F17	HD47
H26	HDSTBP1#
H27	VSS
H28	HD19
H29	HA3#
H30	VSS
H31	HREQ2#
H32	VSS
H33	HD1
H34	VSS
H35	HD4
J1	RSV
J2	VSS
J3	RSV
J4	VSS
J5	RSV
J6	RSV
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	EXP_RXP1
J12	NC
J13	RSV
J14	CRTBLUE#
J15	VSS
J16	VSS
J17	VSS
J18	VSS
J19	HDSTBP2#

Ball	Signal Name DDR
G12	NC
G13	VSS
G14	CRTRED#
G15	VSS
G16	RSV
G17	VSS
G18	HD45
G19	VSS
G20	VSS
G21	VTT
J30	VSS
J31	HADSTB0#
J32	HRS2#
J33	HD0
J34	HD2
J35	HDEFER#
K1	RSV
K2	VSS
K3	RSV
K4	VSS
K5	VSS
K6	VSS
K7	RSV
K8	RSV
K9	VSS
K10	VSS
K11	VSS
K12	NC
K13	RSV
K14	VSS
K15	RSV
K16	EXTTS#
K17	HD44
K18	HD43
K19	HDINV2#
K20	VSS
K21	HD39
K22	HD34
K23	HD31

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 4 of 11)

Ball	Signal Name DDR
H16	BSEL0
H17	NC
H18	HD46
H19	HD41
H20	HD40
H21	VSS
H22	VTT
H23	HD37
H24	VSS
H25	VSS
K34	HRS0#
K35	VSS
L1	RSV
L2	VSS
L3	RSV
L4	VSS
L5	RSV
L6	RSV
L7	VSS
L8	VSS
L9	VSS
L10	VCC
L11	VSS
L12	NC
L13	VSS
L14	CRTDDCDATA
L15	VSS
L16	VSS
L17	VSS
L18	VSS
L19	NC
L20	VSS
L21	VSS
L22	VSS
L23	HD30
L24	VSS
L25	HD29
L26	HA18#
L27	VSS

Ball	Signal Name DDR
J20	VSS
J21	HD35
J22	HD32
J23	VSS
J24	HD33
J25	HD27
J26	HDINV1#
J27	HD21
J28	HA13#
J29	HA5#
M3	RSV
M4	VSS
M5	VSS
M6	VSS
M7	RSV
M8	RSV
M9	VSS
M10	VSS
M11	VSS
M12	DREFCLKN
M13	DREFCLKP
M14	ICH_SYNC#
M15	CRTDDCCLK
M16	RSV
M17	VSS
M18	HD42
M19	HD38
M20	VSS
M21	HD36
M22	HCLKN
M23	HCLKP
M24	VSS
M25	VSS
M26	HA20#
M27	VSS
M28	HA16#
M29	VSS
M30	HA10#
M31	HADS#

Ball	Signal Name DDR
K24	VSS
K25	HD28
K26	VSS
K27	HA14#
K28	VSS
K29	HA4#
K30	HA8#
K31	VSS
K32	VSS
K33	HA15#
N7	VSS
N8	VSS
N9	VSS
N10	VSS
N11	VSS
N12	NC
N13	VCC
N14	VCC
N15	VCC
N16	VCC
N17	VSS
N18	VCC
N19	VSS
N20	VCC
N21	VCC
N22	NC
N23	NC
N24	NC
N25	VSS
N26	HA19#
N27	HADSTB1#
N28	VSS
N29	HA23#
N30	VSS
N31	HA21#
N32	VSS
N33	HA26#
N34	HTRDY#
N35	HHITM#

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 5 of 11)

Ball	Signal Name DDR
L28	HA12#
L29	HA9#
L30	VSS
L31	HA11#
L32	VSS
L33	HLOCK#
L34	HHIT#
L35	HDBSY#
M1	RSV
M2	VSS
P11	VSS
P12	NC
P13	VCC
P14	VCC
P15	VCC
P16	VSS
P17	VCC
P18	VSS
P19	VCC
P20	VSS
P21	VCC
P22	VCC
P23	NC
P24	NC
P25	VSS
P26	HA22#
P27	VSS
P28	HA24#
P29	VSS
P30	NC
P31	VSS
P32	VSS
P33	HEDRDY#
P34	HRS1#
P35	VSS
R1	RSV
R2	VSS
R3	DMI_TXP0
R4	VSS

Ball	Signal Name DDR
M32	HDRDY#
M33	–
M34	VSS
M35	HBNR#
N1	RSV
N2	VSS
N3	RSV
N4	VSS
N5	RSV
N6	RSV
R15	VCC
R16	VCC
R17	VSS
R18	VCC
R19	VSS
R20	VCC
R21	VSS
R22	VCC
R23	VCC
R24	NC
R25	VSS
R26	VSS
R27	VSS
R28	HA25#
R29	HA17#
R30	SCB_A4
R31	SCB_A5
R32	SDQ_A58
R33	HBREQ0#
R34	SDQ_A59
R35	RSV
T1	DMI_TXP1
T2	VSS
T3	DMI_TXN0
T4	VSS
T5	VSS
T6	VSS
T7	VSS
T8	DMI_RXN1

Ball	Signal Name DDR
P1	RSV
P2	VSS
P3	RSV
P4	VSS
P5	VSS
P6	VSS
P7	RSV
P8	RSV
P9	VSS
P10	RSV
T19	VCC
T20	VCC
T21	VCC
T22	VSS
T23	VCC
T24	VCC
T25	VSS
T26	HA30#
T27	HA27#
T28	VSS
T29	HA31#
T30	VSS
T31	HA28#
T32	VSS
T33	SDQ_A62
T34	VSS
T35	SDQ_A63
U1	DMI_TXN1
U2	VSS
U3	DMI_TXP2
U4	VSS
U5	DMI_RXP0
U6	DMI_RXN0
U7	VSS
U8	VSS
U9	VSS
U10	DMI_RXN3
U11	VSS
U12	NC

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 6 of 11)

Ball	Signal Name DDR
R5	RSV
R6	RSV
R7	VSS
R8	VSS
R9	VSS
R10	RSV
R11	VSS
R12	NC
R13	VCC
R14	VCC
U23	VSS
U24	VCC
U25	VSS
U26	SDQ_B63
U27	VSS
U28	HA29#
U29	VSS
U30	RSV (SDQS_A8#)
U31	VSS
U32	VSS
U33	SDM_A7
U34	SDQS_A7
U35	RSV (SDQS_A7#)
V1	VSS
V2	VSS
V3	DMI_TXN2
V4	VSS
V5	DMI_TXP3
V6	VSS
V7	DMI_RXP2
V8	DMI_RXN2
V9	VSS
V10	DMI_RXP3
V11	VSS
V12	NC
V13	VCC
V14	VCC
V15	VCC
V16	VSS

Ball	Signal Name DDR
T9	DMI_RXP1
T10	VSS
T11	VSS
T12	NC
T13	VCC
T14	VCC
T15	VCC
T16	VCC
T17	VCC
T18	VSS
V27	VSS
V28	SDQ_B58
V29	SDQ_B59
V30	SDQS_A8
V31	SCB_A1
V32	SCB_A0
V33	SDQ_A57
V34	SDQ_A56
V35	VSS
W1	VCC_EXP
W2	VCC_EXP
W3	VCC_EXP
W4	VCC_EXP
W5	DMI_TXN3
W6	VCC_EXP
W7	VCC_EXP
W8	VCC_EXP
W9	VCC_EXP
W10	EXP_COMPI
W11	VSS
W12	NC
W13	VCC
W14	VCC
W15	VSS
W16	VCC
W17	VSS
W18	VCC
W19	VSS
W20	VCC

Ball	Signal Name DDR
U13	VCC
U14	VCC
U15	VSS
U16	VCC
U17	VSS
U18	VCC
U19	VSS
U20	VCC
U21	VSS
U22	VCC
W31	SDM_B7
W32	VSS
W33	SDQ_A61
W34	SDQ_A51
W35	SDQ_A60
Y1	VCC_EXP
Y2	VCC_EXP
Y3	VCC_EXP
Y4	VCC_EXP
Y5	VCC_EXP
Y6	VCC_EXP
Y7	VCC_EXP
Y8	VCC_EXP
Y9	VCC_EXP
Y10	EXP_COMPO
Y11	VSS
Y12	NC
Y13	VCC
Y14	VCC
Y15	VCC
Y16	VCC
Y17	VCC
Y18	VSS
Y19	VCC
Y20	VCC
Y21	VCC
Y22	VSS
Y23	VCC
Y24	VCC

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 7 of 11)

Ball	Signal Name DDR
V17	VCC
V18	VSS
V19	VCC
V20	VSS
V21	VCC
V22	VSS
V23	VCC
V24	VCC
V25	VSS
V26	VSS
Y35	SDQ_A55
AA1	VSS
AA2	VSS
AA3	VSS
AA4	VSS
AA5	VSS
AA6	VSS
AA7	VSS
AA8	VSS
AA9	VSS
AA10	VSS
AA11	VSS
AA12	NC
AA13	VCC
AA14	VCC
AA15	VSS
AA16	VCC
AA17	VSS
AA18	VCC
AA19	VSS
AA20	VCC
AA21	VCC
AA22	VCC
AA23	VCC
AA24	VCC
AA25	VSS
AA26	VSS
AA27	VSS
AA28	SDQ_B56

Ball	Signal Name DDR
W21	VSS
W22	VCC
W23	VSS
W24	VCC
W25	VSS
W26	SDQ_B62
W27	SDQS_B7
W28	VSS
W29	SDQ_B57
W30	VSS
AB4	VCC
AB5	VCC
AB6	VCC
AB7	VCC
AB8	VCC
AB9	VCC
AB10	VCC
AB11	VCC
AB12	NC
AB13	VCC
AB14	VCC
AB15	VCC
AB16	VCC
AB17	VCC
AB18	VCC
AB19	VCC
AB20	VCC
AB21	VCC
AB22	VCC
AB23	VCC
AB24	VCC
AB25	VSS
AB26	SDQ_B51
AB27	SDQ_B55
AB28	VSS
AB29	SCB_A7
AB30	VSS
AB31	SDQS_B6
AB32	VSS

Ball	Signal Name DDR
Y25	VSS
Y26	SDQ_B60
Y27	VSS
Y28	RSV (SDQS_B7#)
Y29	VSS
Y30	SCB_A6
Y31	VSS
Y32	VSS
Y33	SDQ_A50
Y34	VSS
AC8	VCC
AC9	VCC
AC10	VCC
AC11	VCC
AC12	RSV
AC13	RSV
AC14	RSV
AC15	RSV
AC16	RSV
AC17	RSV
AC18	RSV
AC19	RSV
AC20	RSV
AC21	RSV
AC22	RSV
AC23	NC
AC24	NC
AC25	VSS
AC26	SDQ_B50
AC27	VSS
AC28	SDQ_B54
AC29	VSS
AC30	RSV (SDQS_B6#)
AC31	VSS
AC32	VSS
AC33	SCLK_A2#
AC34	SCLK_A5#
AC35	SCLK_A5
AD1	VCC

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 8 of 11)

Ball	Signal Name DDR
AA29	SDQ_B61
AA30	SCB_A3
AA31	SCB_A2
AA32	SDQ_A54
AA33	SDM_A6
AA34	SDQS_A6
AA35	RSV (SDQS_A6#)
AB1	VCC
AB2	VCC
AB3	VCC
AD12	SDQ_B20
AD13	VSS
AD14	SDQ_B17
AD15	SDQ_B29
AD16	VSS
AD17	SDQ_A29
AD18	SDQ_B24
AD19	VSS
AD20	VSS
AD21	NC
AD22	VSS
AD23	SDQ_B37
AD24	SDM_B6
AD25	VSS
AD26	VSS
AD27	SDQ_A35
AD28	SCLK_B5#
AD29	SCLK_B5
AD30	NC
AD31	SDQ_A48
AD32	SMA_B13
AD33	–
AD34	VSS
AD35	SDQ_A49
AE1	SDQ_A5
AE2	SDQ_A4
AE3	SDQ_A0
AE4	VSS
AE5	RSV (SOCOMP1)

Ball	Signal Name DDR
AB33	SMA_A13
AB34	SCLK_A2
AB35	VSS
AC1	VCC
AC2	VCC
AC3	VCC
AC4	VCC
AC5	VCC
AC6	VCC
AC7	VCC
AE16	RSV_TP0
AE17	SDQ_A24
AE18	NC
AE19	SDQ_B25
AE20	SDM_B3
AE21	VSS
AE22	VSS
AE23	VSS
AE24	VSS
AE25	SCLK_B2#
AE26	SCLK_B2
AE27	SDQ_B49
AE28	VSS
AE29	SDQ_B53
AE30	NC
AE31	SDQ_B52
AE32	VSS
AE33	SDQ_A43
AE34	SDQ_A53
AE35	SDQ_A52
AF1	VSS
AF2	SDM_A0
AF3	SDQ_A1
AF4	VSS
AF5	RSV (SOCOMP0)
AF6	VSS
AF7	RSTIN#
AF8	VSS
AF9	SM_SLEWIN1

Ball	Signal Name DDR
AD2	VCC
AD3	VCC
AD4	VCC
AD5	VCC
AD6	VCC
AD7	VCC
AD8	VCC
AD9	VCC
AD10	VCC
AD11	VSS
AF20	RSV (SDQS_B3#)
AF21	VSS
AF22	NC
AF23	SDQ_B36
AF24	SDQ_B32
AF25	SDM_B4
AF26	VSS
AF27	SDQ_B48
AF28	SDQ_A39
AF29	VSS
AF30	SDQ_B43
AF31	VSS
AF32	VSS
AF33	SDQ_A42
AF34	SDQ_A47
AF35	VSS
AG1	SDQS_A0
AG2	RSV (SDQS_A0#)
AG3	SDQ_A6
AG4	SRCOMP0
AG5	VSS
AG6	NC
AG7	PWROK
AG8	SRCOMP1
AG9	VSS
AG10	SDQ_B1
AG11	SDQ_B0
AG12	VSS
AG13	VSS

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 9 of 11)

Ball	Signal Name DDR
AE6	VSS
AE7	SVREF0
AE8	SVREF1
AE9	VSS
AE10	SM_SLEWOUT1
AE11	SDQ_B4
AE12	VSS
AE13	SDQ_B21
AE14	SDQ_B19
AE15	SDQ_A28
AG24	SDQ_B33
AG25	NC
AG26	RSV (SDQS_B4#)
AG27	SDQ_A38
AG28	SDQ_B47
AG29	NC
AG30	SDQ_B46
AG31	SDQ_B42
AG32	SDQ_A46
AG33	RSV (SDQS_A5#)
AG34	SDM_A5
AG35	SDQS_A5
AH1	VSS
AH2	SDQ_A7
AH3	SDQ_A2
AH4	SDQ_B12
AH5	NC
AH6	VSS
AH7	SDQ_B7
AH8	SDQS_B0
AH9	RSV (SDQS_B0#)
AH10	SDM_B0
AH11	VSS
AH12	SDM_B2
AH13	SDQS_B2
AH14	VSS
AH15	RSV_TP1
AH16	SDQS_A3
AH17	SDQ_A27

Ball	Signal Name DDR
AF10	VSS
AF11	SDQ_B5
AF12	SDQ_B11
AF13	SDQ_B16
AF14	SDQ_B18
AF15	SDQ_B28
AF16	SDQ_A25
AF17	SDM_A3
AF18	VSS
AF19	NC
AH28	SDQS_B5
AH29	VSS
AH30	RSV (SDQS_B5#)
AH31	SDM_B5
AH32	VSS
AH33	VSS
AH34	SDQ_A40
AH35	SDQ_A41
AJ1	SDQ_A12
AJ2	SDQ_A3
AJ3	SDQ_A13
AJ4	VSS
AJ5	SDQ_B13
AJ6	SDQ_B3
AJ7	SDQ_B2
AJ8	SDQ_B6
AJ9	VSS
AJ10	VSS
AJ11	SCLK_B1#
AJ12	SM_SLEWIN0
AJ13	VSS
AJ14	NC
AJ15	VSS
AJ16	VSS
AJ17	SDQ_A31
AJ18	SCB_B1
AJ19	VSS
AJ20	SCB_B0
AJ21	RSV (SDQS_B8#)

Ball	Signal Name DDR
AG14	RSV (SDQS_B2#)
AG15	VSS
AG16	VSS
AG17	RSV (SDQS_A3#)
AG18	VSS
AG19	VSS
AG20	SDQS_B3
AG21	VSS
AG22	VSS
AG23	SCLK_B0#
AJ32	VSS
AJ33	SDM_A4
AJ34	SDQ_A45
AJ35	VSS
AK1	VSS
AK2	SDQ_A8
AK3	SDQ_A9
AK4	VSS
AK5	SDM_B1
AK6	VSS
AK7	SDQ_A17
AK8	VSS
AK9	SCLK_B4
AK10	SDQ_B8
AK11	VSS
AK12	SM_SLEWOUT0
AK13	SDQ_B22
AK14	VSS
AK15	RSV_TP3
AK16	SDQ_A30
AK17	VSS
AK18	SCB_B5
AK19	SDQ_B27
AK20	VSS
AK21	SDQS_B8
AK22	SCLK_B3#
AK23	VSS
AK24	NC
AK25	VSS

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 10 of 11)

Ball	Signal Name DDR
AH18	VSS
AH19	SDQ_B30
AH20	VSS
AH21	SDQ_B31
AH22	VSS
AH23	SCLK_B0
AH24	NC
AH25	SDQS_B4
AH26	VSS
AH27	SDQ_A34
AL1	SDM_A1
AL2	RSV (SDQS_A1#)
AL3	SDQS_A1
AL4	SDQ_B9
AL5	RSV (SDQS_B1#)
AL6	SDQ_B14
AL7	SDQ_A19
AL8	SDQ_B10
AL9	SCLK_B4#
AL10	VSS
AL11	SCLK_B1
AL12	VCCSM
AL13	VSS
AL14	SDQ_B23
AL15	RSV_TP2
AL16	VSS
AL17	SDQ_A26
AL18	SDQ_B26
AL19	VSS
AL20	SCB_B4
AL21	SCB_B6
AL22	SCB_B7
AL23	SCLK_B3
AL24	VSS
AL25	SDQ_B38
AL26	SDQ_B34
AL27	NC
AL28	SCLK_A0#
AL29	SCLK_A3#

Ball	Signal Name DDR
AJ22	VSS
AJ23	SCB_B2
AJ24	SCB_B3
AJ25	SDQ_B39
AJ26	SDQ_B35
AJ27	VSS
AJ28	RSV (SDQS_A4#)
AJ29	SDQ_B44
AJ30	VSS
AJ31	SDQ_B41
AM5	SDQS_B1
AM6	VSS
AM7	SDQ_A22
AM8	SDQ_A23
AM9	SDQ_A18
AM10	VCCSM
AM11	VCCSM
AM12	NC
AM13	VCCSM
AM14	VCCSM
AM15	NC
AM16	VCCSM
AM17	VCCSM
AM18	NC
AM19	VCCSM
AM20	VCCSM
AM21	NC
AM22	VCCSM
AM23	VCCSM
AM24	NC
AM25	VCCSM
AM26	VCCSM
AM27	VCCSM
AM28	VSS
AM29	VCCSM
AM30	SCLK_A3
AM31	VSS
AM32	VCCSM
AM33	SCS_A0#

Ball	Signal Name DDR
AK26	VSS
AK27	SDQS_A4
AK28	SCLK_A0
AK29	SDQ_A32
AK30	VSS
AK31	SDQ_A33
AK32	SDQ_B40
AK33	SDQ_B45
AK34	SDQ_A44
AK35	VCCSM
AN9	SCKE_A1
AN10	SCKE_A3
AN11	SMA_B12
AN12	–
AN13	SMA_B8
AN14	SMA_B5
AN15	SMA_A9
AN16	SMA_A7
AN17	SMA_B2
AN18	SMA_A8
AN19	SMA_B0
AN20	SMA_A6
AN21	SMA_A3
AN22	SMA_A1
AN23	SMA_A0
AN24	–
AN25	NC
AN26	SBS_A1
AN27	SWE_B#
AN28	SBS_A0
AN29	NC
AN30	SWE_A#
AN31	NC
AN32	NC
AN33	SCS_B0#
AN34	SCS_B3#
AN35	VCCSM
AP1	NC
AP2	SDQ_A14

Table 13-4. Intel® E7221 MCH DDR Signal List by Ball (Sheet 11 of 11)

Ball	Signal Name DDR
AL30	SDQ_A36
AL31	SDQ_A37
AL32	VSS
AL33	SCS_A2#
AL34	SCAS_A#
AL35	SCS_A1#
AM1	–
AM2	SCLK_A1
AM3	SCLK_A1#
AM4	VSS
AP13	SMA_A12
AP14	SMA_B7
AP15	SMA_A11
AP16	VCCSM
AP17	SMA_B6
AP18	SMA_B1
AP19	SMA_A5
AP20	VCCSM
AP21	SMA_A4
AP22	SMA_A2
AP23	RSV (SBS_A2)
AP24	VCCSM
AP25	NC
AP26	SBS_B0
AP27	SRAS_B#
AP28	VCCSM
AP29	SRAS_A#
AP30	NC
AP31	NC
AP32	NC

Ball	Signal Name DDR
AM34	SCS_A3#
AM35	–
AN1	VSS
AN2	SCLK_A4
AN3	SCLK_A4#
AN4	SDQ_A10
AN5	SDQ_A21
AN6	SDQ_B15
AN7	RSV (SDQS_A2#)
AN8	SCKE_B1
AP33	SCS_B2#
AP34	SCS_B1#
AP35	NC
AR1	NC
AR2	NC
AR3	VSS
AR4	–
AR5	SDQ_A20
AR6	VSS
AR7	VCCSM
AR8	SCKE_B3
AR9	SCKE_B2
AR10	VCCSM
AR11	SCKE_A0
AR12	SMA_B9
AR13	VSS
AR14	VCCSM
AR15	SMA_B4
AR16	SMA_B3

Ball	Signal Name DDR
AP3	SDQ_A15
AP4	SDQ_A11
AP5	SDQ_A16
AP6	SDM_A2
AP7	SDQS_A2
AP8	VCCSM
AP9	SCKE_B0
AP10	SCKE_A2
AP11	SMA_B11
AP12	VCCSM
AR17	VSS
AR18	VCCSM
AR19	SBS_B1
AR20	SMA_B10
AR21	VSS
AR22	VCCSM
AR23	SMA_A10
AR24	RSV (SBS_B2)
AR25	VSS
AR26	VCCSM
AR27	SCAS_B#
AR28	NC
AR29	NC
AR30	VSS
AR31	VCCSM
AR32	–
AR33	VCCSM
AR34	NC
AR35	NC

13.5 Package Information

The MCH package measures 37.5 mm × 37.5 mm. The 1092 balls are located in a non-grid pattern. For example, the ball pitch varies from 31.8 mils to 43.0 mils depending upon the X-axis or Y-axis direction. Refer to Figure 13-5 and Figure 13-6.

Figure 13-5. Intel® E7221 MCH Package Dimensions

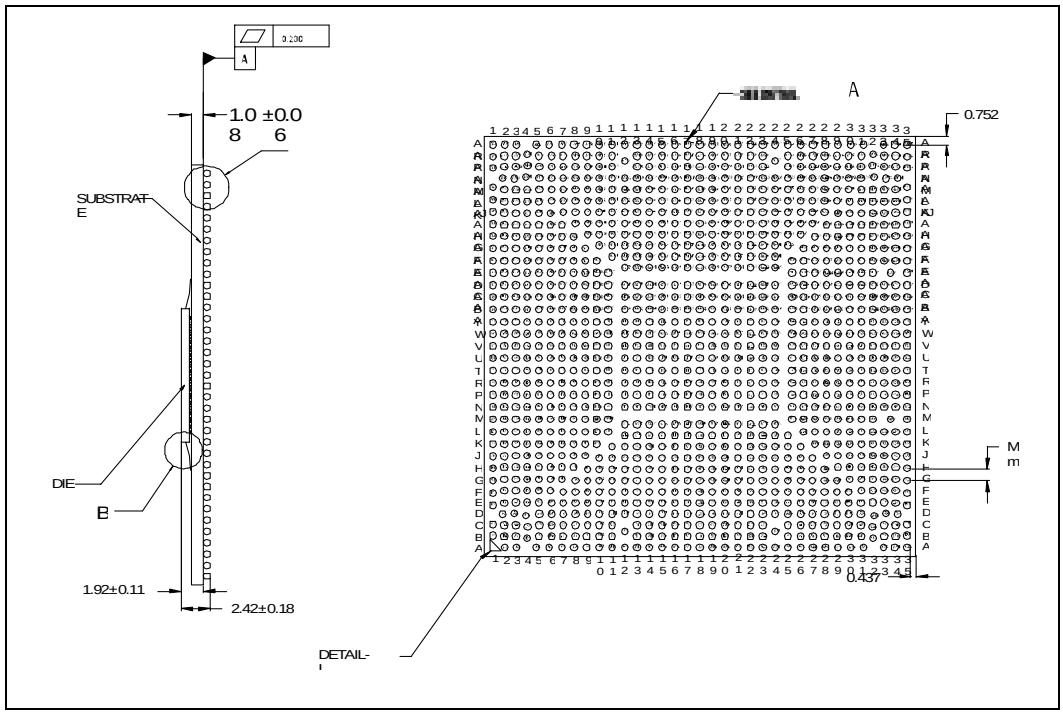
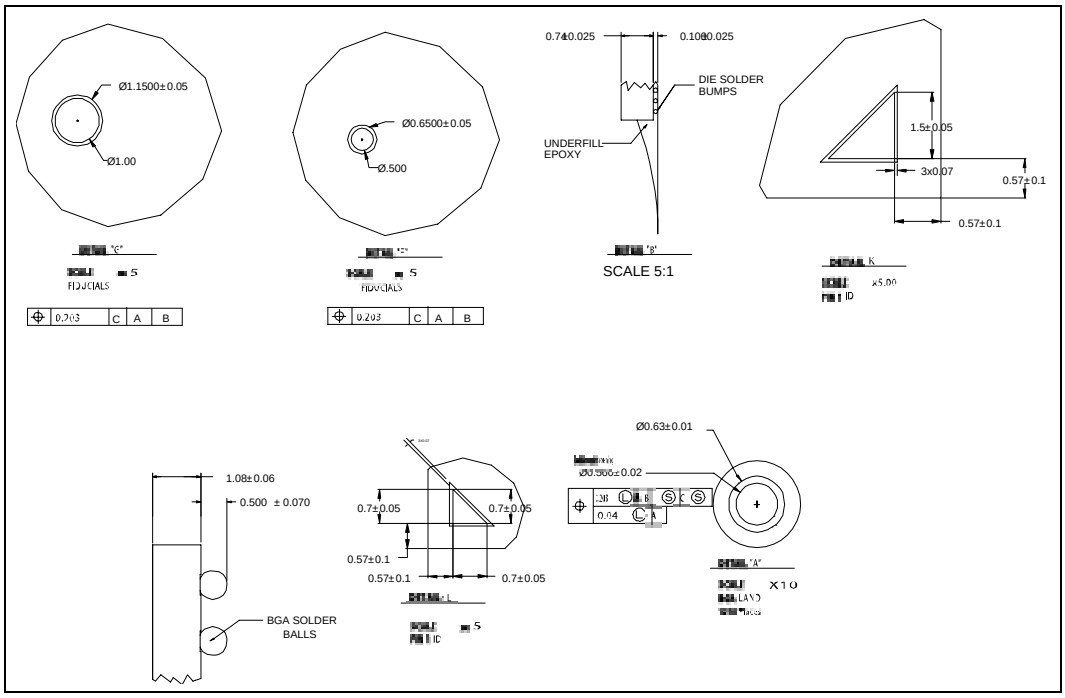


Figure 13-6. Intel® E7221 MCH Package Detail



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